Contract No. FA64WA-5223

IBM Field Engineering Maintenance Diagrams

7201-02 Computing Element

SFN-0202-1

PREFACE

This manual contains the maintenance-oriented and recall diagrams referenced in the companion 7201-02 Computing Element FETOM (Form SFN-0201) and in the 7201-02 Computing Element FEMM (Form SFN-0203).

The diagrams in this manual are arranged into six categories:

Category 1. Diagnostic Techniques
Category 2. Overall Data Flow
Category 3. Data Flow by Instruction Class
Category 4. Functional Units
Category 5. Operations
Category 6. Manual Controls and Maintenance Facilities

All diagrams are in numerical order. The first digit of the diagram number reflects the category; for example, Diagram 4-210 belongs to Category 4, Functional Units. A category may be further subdivided into functional groups; for example, in Category 4, the diagrams have been grouped as follows:

Group 1. Timing and Clock Control
Group 2. ROS
Group 3. Data and Control Registers
Group 4. Local Storage
Group 5. Serial and Parallel Adders
Group 6. Status and Control Triggers
Group 7. SCI

Prerequisite and companion manuals are:

Prerequisite Manuals

9020E System Introduction, Theory of Operation Manual, Form SFN-0103
9020D System Introduction, Theory of Operation Manual, Form SFN-0104

Companion Manuals

7201-02 Computing Element, Theory of Operation Manual, Form SFN-0201
7201-02 Computing Element, Maintenance Manual, Form SFN-0203
7201-02 Computing Element, Installation Manual, Form SFN-0204
7201-02 Parts Catalog, Form SFN-0205
9020 D/E Power Controls and Distribution, Theory of Operation Manual, Form SFN-0105.

First Edition (July, 1970)

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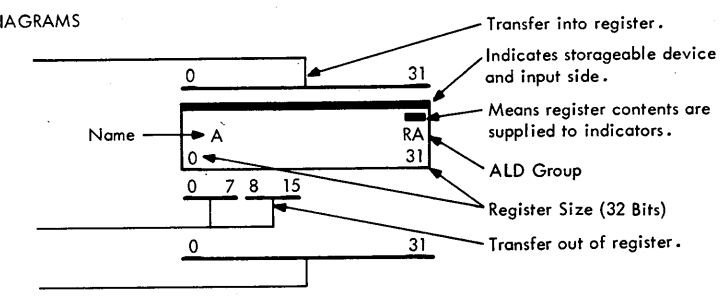
*Note: 1052 Adapter is used only with the 9020E configuration.

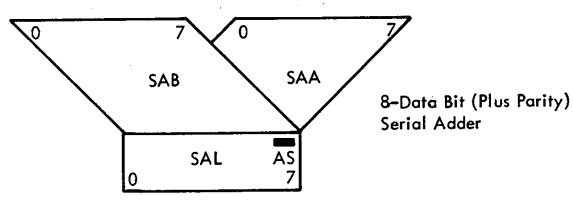
ABBREVIATIONS

ABC	AB register byte counter
ac	alternating current
ACR	Automatic Carrier Return
adr	address, addressed, addressing
ALD	automated logic diagram
ALTN	Alternate
amp	ampere
APSA	alternate preferential storage area
ASC	address store compare
ATC	air traffic control
ATN	alternate test number
ATR	address translation register
Attn	attention
Aux	Auxiliary Magnet
BCD	binary-coded decimal
BCU	bus control unit (alternate terminology for SCI)
BL	blink
BR	brightness
BSM	basic storage module
C	capacitor
CAS	control automation system
CAW	channel address word
CB	circuit breaker
CC	condition code, also Configuration Console
CCC	Central Computer Complex
CCR	configuration control register
CCW	channel command word
CE	Computing Element
Charistic	Characteristic
CLD	control automation system logic diagram
Cmd	command
CPU	Central Processing Unit (alternate terminology for CE)
CR	diode or Carrier Return
CROS	capacitive read-only storage
CSW	channel status word
CT	conditional terminate
CTC	channel-to-channel
CU	Control Unit
CVG	Character Vector Generator
DA	dash
DAR	diagnose accessible register
DARM	diagnose accessible register mask
DAU	Data Adapter Unit
dc	direct current
DCP	Display Channel Processor
DE	Display Element
dec	decimal
dec div	decimal divide
dec ovflo	decimal overflow
DG	Display Generator
Disc	disconnect
dly	delay
Dply	display
dsbl	disable
DX	first byte in a series of destination bytes
DX+1	second byte in a series of destination bytes
DX+2	third byte in a series of destination bytes
ELC	element check
end op	end operation
EOB	end of block
EOL	End-of-Line
EPO	emergency power off
ERSLT	expected result
EXC	Executive Control Program
exp ovflo	exponent overflow
exp unflo	exponent underflow
F	fuse
FEMDM	Field Engineering Maintenance Diagrams Manual
FEMI	Field Engineering Manual of Instruction
FEMM	Field Engineering Maintenance Manual
FETOM	Field Engineering Theory of Operation Manual
fix-pt ovflo	fixed-point overflow
FLT	fault locating test
flt-pt div	floating-point divide
FMTN	Format New
FMTO	Format Old
FMTW	Format Weather
FPR	Floating-point register
fract	fraction

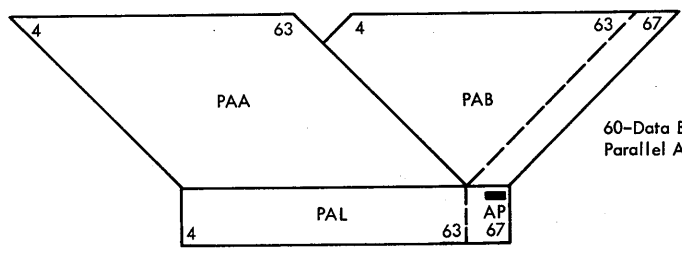
GIS	general initialization sequence
GPR	general-purpose register
hex	hexadecimal
Hz	Hertz
IC	instruction counter
ICR	inhibit carrier return
IDES	inhibit display element stop
I-Fetch	instruction fetching
ILC	instruction length code
ILOS	inhibit logout stop
Init	initial
I/O	input/output
IOCE	Input/Output Control Element
IPL	initial program load
K	kilo; also relay
kHz	kilohertz
LAB	logical address bus
LADS	Logic Automation Documentation System
LAL	local storage address latches
LAR	local storage address register
LC	lower case
LF	line feed
LOS	logout stop
LS	local store
LSWR	local storage working register
MACH	maintenance and channel (storage)
max	maximum
MC	machine check
MCW	maintenance control word
mHz	megahertz
MMSC	maintenance mode stop clock
Mple	Multiple
MPR	multiplier
MPX	multiplex
ms	millisecond
NDT	new descriptor tables
no op	no operation
NRM	new refresh memory
NRMA	new refresh memory address
ns	nanosecond
OBS	on battery signal
ODT	old descriptor tables
op code	operation code
oper	operation
opr	operand
ORM	old refresh memory
ORMA	old refresh memory address
OTC	out of tolerance check
P	parity
PAA	parallel adder A-side
PAB	parallel adder B-side
PAL	parallel adder latch
PB	pushbutton
pf	picofarad
PK	power contactor
PP	partial product
PQ	partial quotient
priv oper	privileged operation
proc	process
prog	program
PROSAR A	previous read-only storage address register A
PROSAR B	previous read-only storage address register B
prot	protection
PS	power supply
PSA	preferential storage address
PSBA	preferential storage base address
PSBAR	preferential storage base address register
PSW	program status word
PVD	Plan View Display
R	resistor
RCU	Reconfiguration Control Unit
reg	register
RKM	Radar Keyboard Multiplexor
ROS	read-only storage
ROSAR	read-only storage address register
ROSBR	read-only storage backup register
ROSDR	read-only storage data register
RST	Reset
SAA	serial adder A-side
SAB	storage address bus, also serial adder B-side
SAL	serial adder latch
SATR	set Address Translation Register
SBA	serial adder bus A
SBB	serial adder bus B
SC	System Console
SCI	storage control interface
SCON	set Configuration Control Register
SCOPEX	scoping index
SCR	silicon-controlled rectifier
SDBI	storage data bus in
SDBO	storage data bus out
SE	Storage Element
Sel	select
Serv	service
signif	significance
SLT	solid logic technology
SMMC	system maintenance monitor console
SMS	standard modular system
SOROS	scan out read-only storage
spec	specification
SRL	Systems Reference Library
SSU	storage switching unit
STAT	status trigger
STC	ST register byte counter
stg	storage
SU	switch unit
sync	synchronizing
T	transformer
TC	time clock (interval timer)
TCU	tape control unit
T(DX)	table byte specified by DX
T(DX+1)	table byte specified by DX+1
TIC	transfer in channel
TN	test number
T/R	tilt/rotate
TU	tape unit
uc	upper case
uf	microfarad
usec	microsecond
UT	unconditional terminate
V	volt
VFL	variable-field length
VFR	visual flight rules
Xlat	translate
$\geq$	greater than or equal to
$\geqq$	greater than or equal to
$\leq$	less than or equal to
$\leqq$	less than or equal to
=	equal to
$\neq$	not equal to
&	and

LOGIC DIAGRAMS

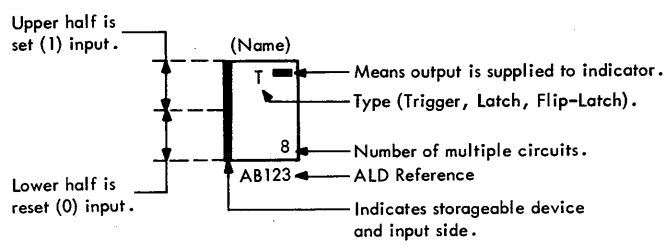


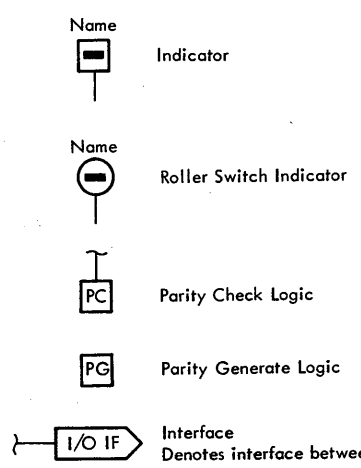


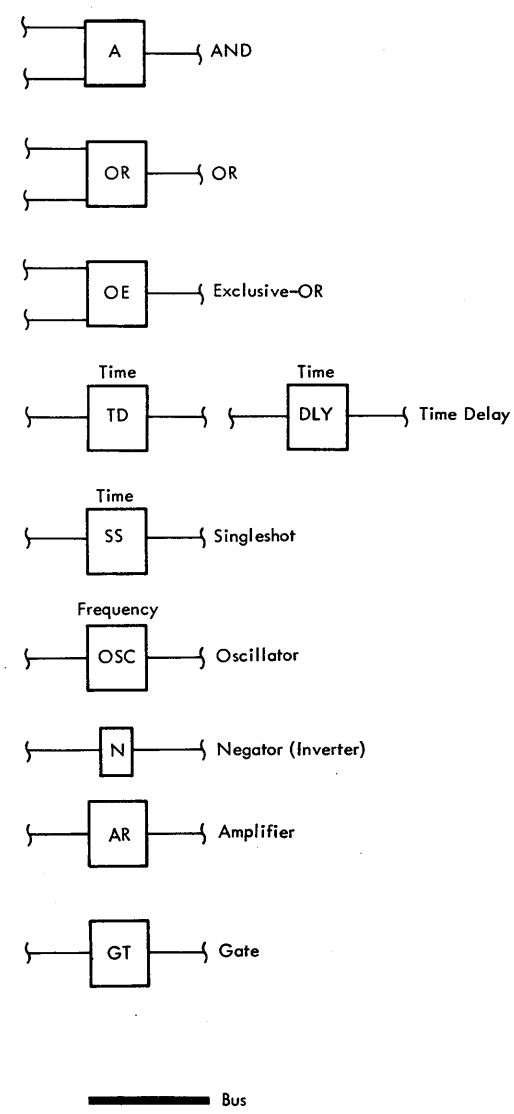
8-Data Bit (Plus Parity) Serial Adder

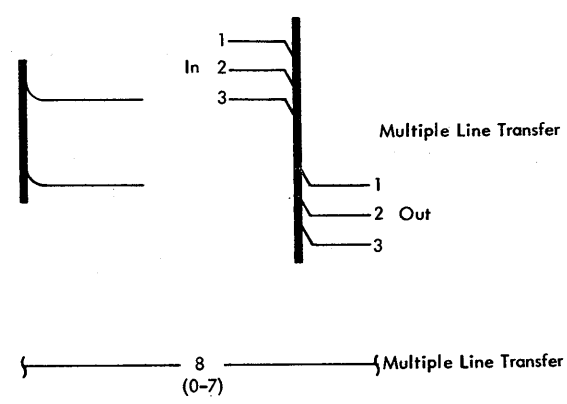


60-Data Bit (Plus Parity) Parallel Adder

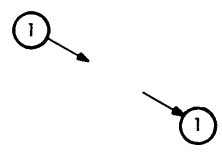








GENERAL

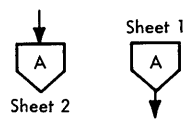


On-Page Connector

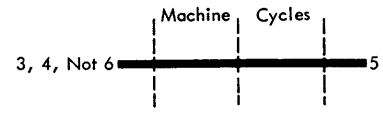
Indicates connection between two parts of the same diagram. Arrow leaving symbol points (line of sight) to correspondingly-numbered symbol.

Off-Page Connector

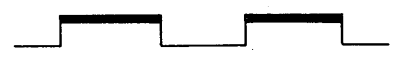
Indicates connection between sheets of the same diagram.



TIMING CHARTS

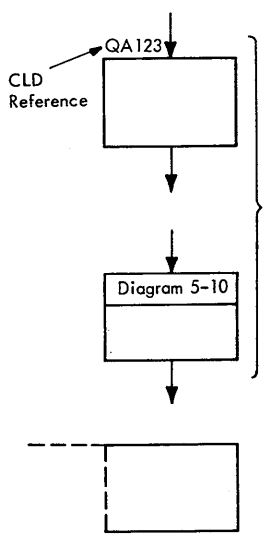


Heavy bar indicates active state. Number(s) at beginning and end of the bar identify the signal(s) (also on the same chart) that activate and deactivate this line. "Not" preceding a number means that the deactive signal conditions this line.



Waveshape
Heavy bar indicates active state.

FLOWCHARTS

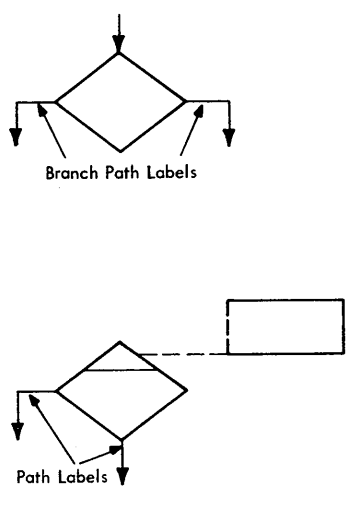


Processing Block

Reference within stripe specifies detailed flowchart of the process.

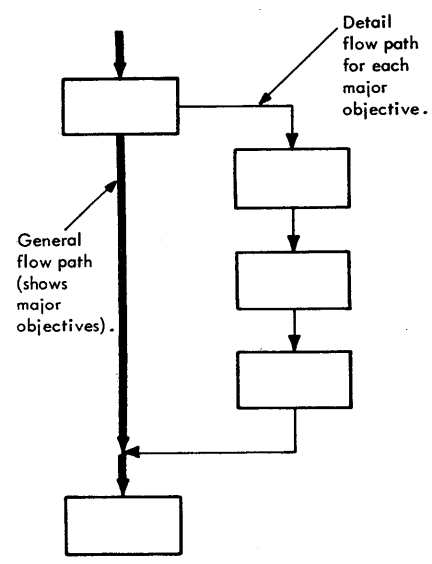
Annotation

Gives descriptive comment or explanatory note.



Decision Block

Indicates point in flowchart where branch to alternate paths is possible. Diagram reference within annotation block connected to stripe specifies detailed flowchart of the decision.



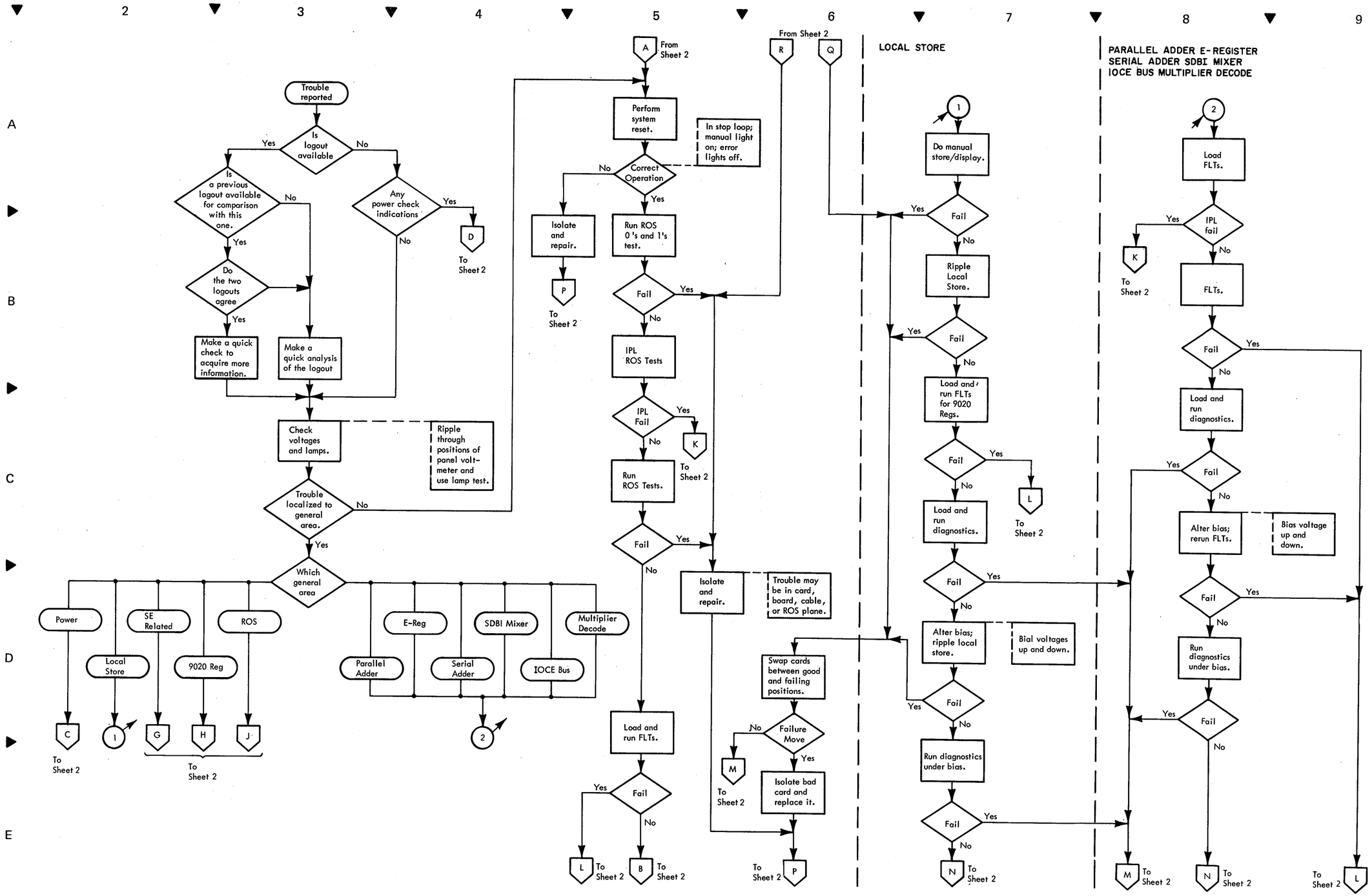


Diagram 1-1. Maintenance Strategy Diagram (Sheet 1 of 2)

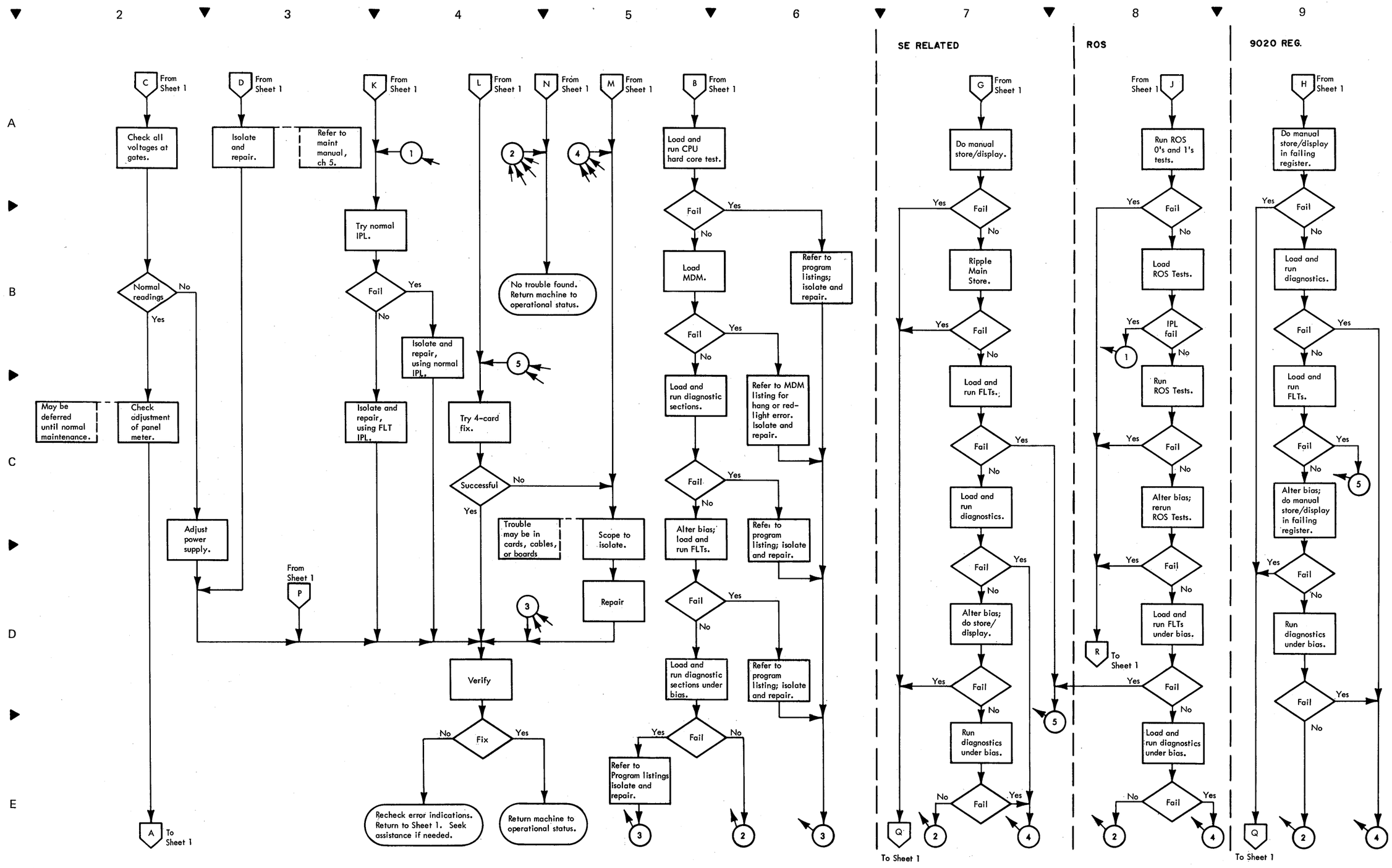


Diagram 1-1. Maintenance Strategy Diagram (Sheet 2 of 2)

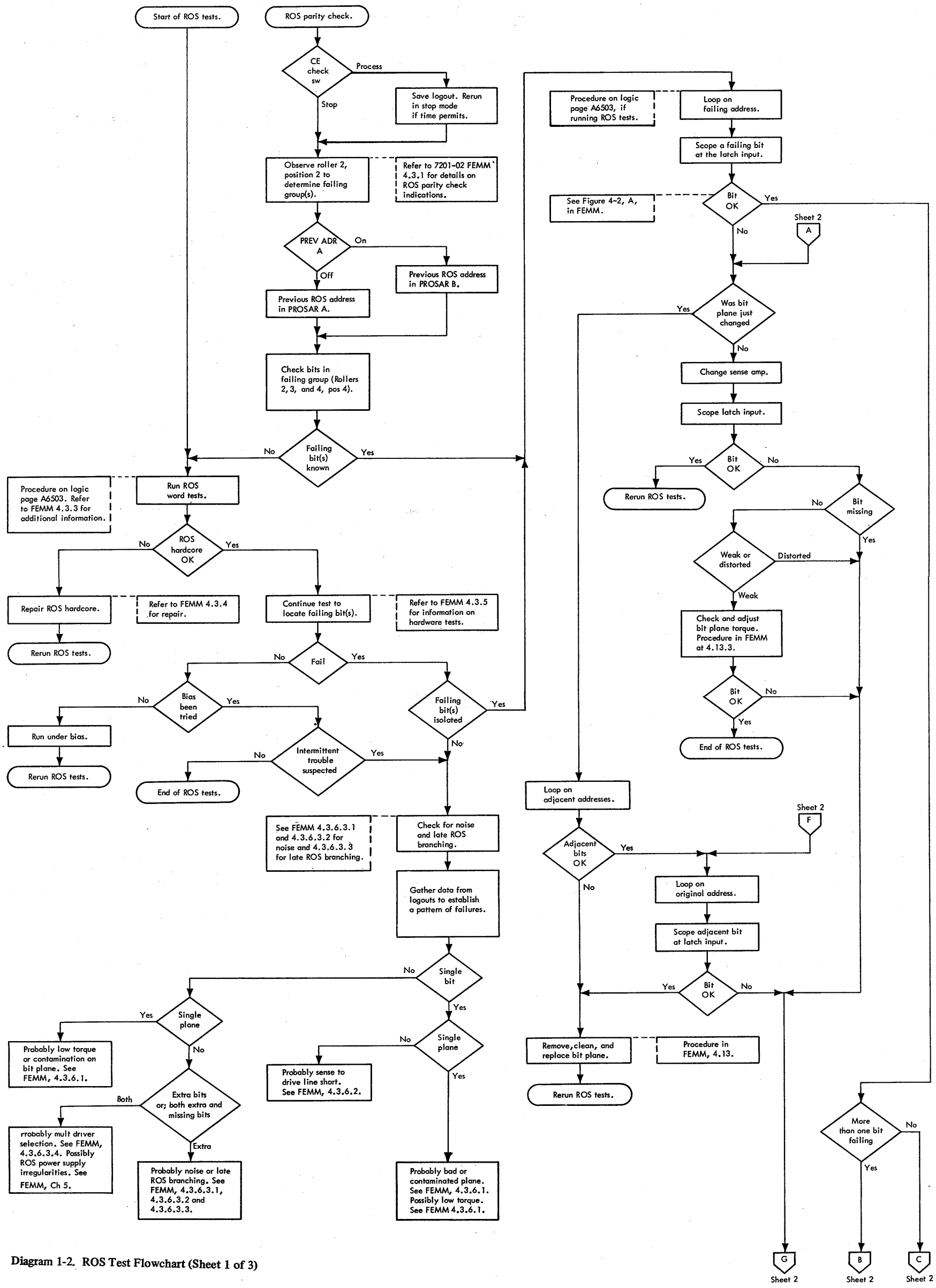


Diagram 1-2. ROS Test Flowchart (Sheet 1 of 3)

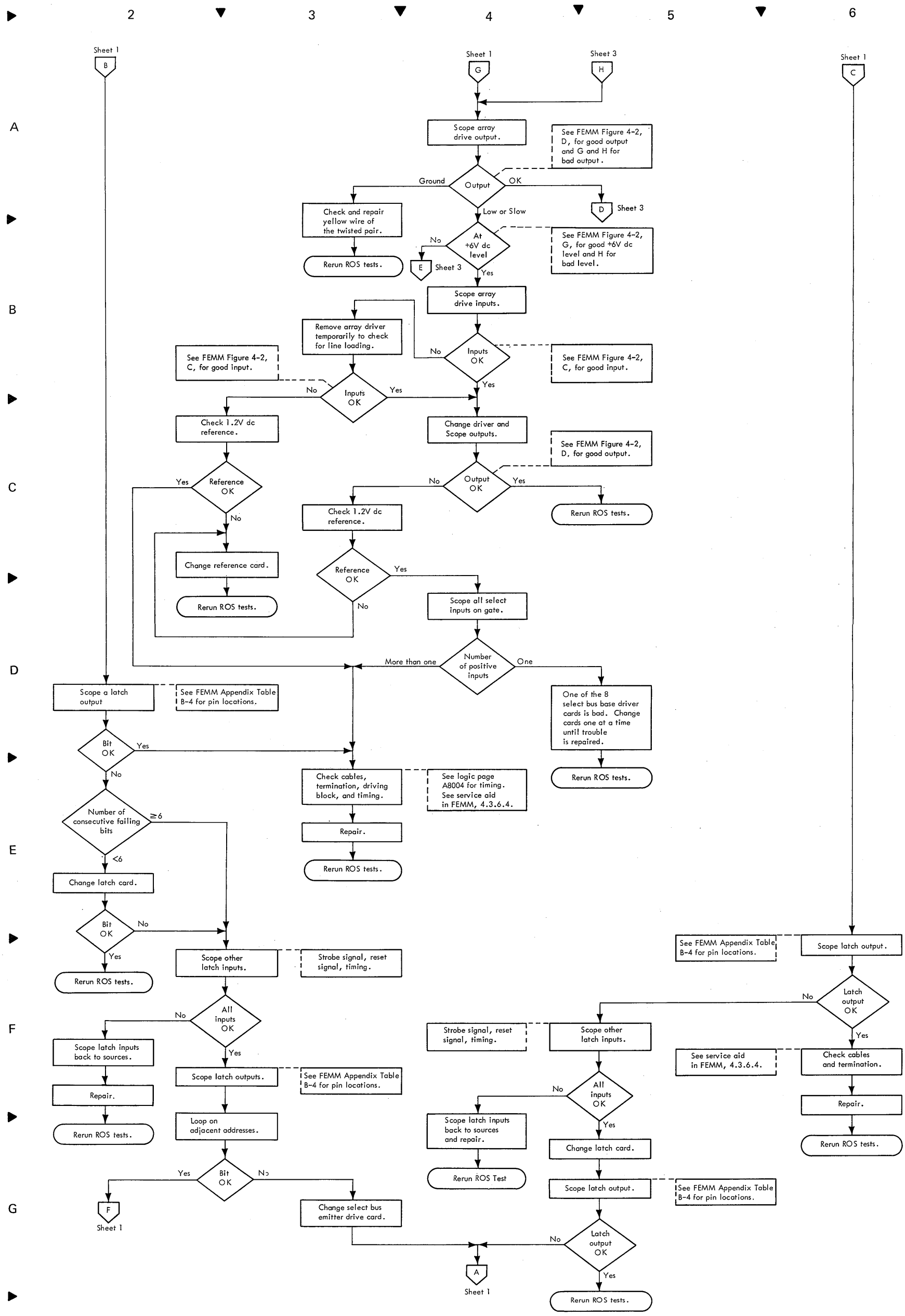
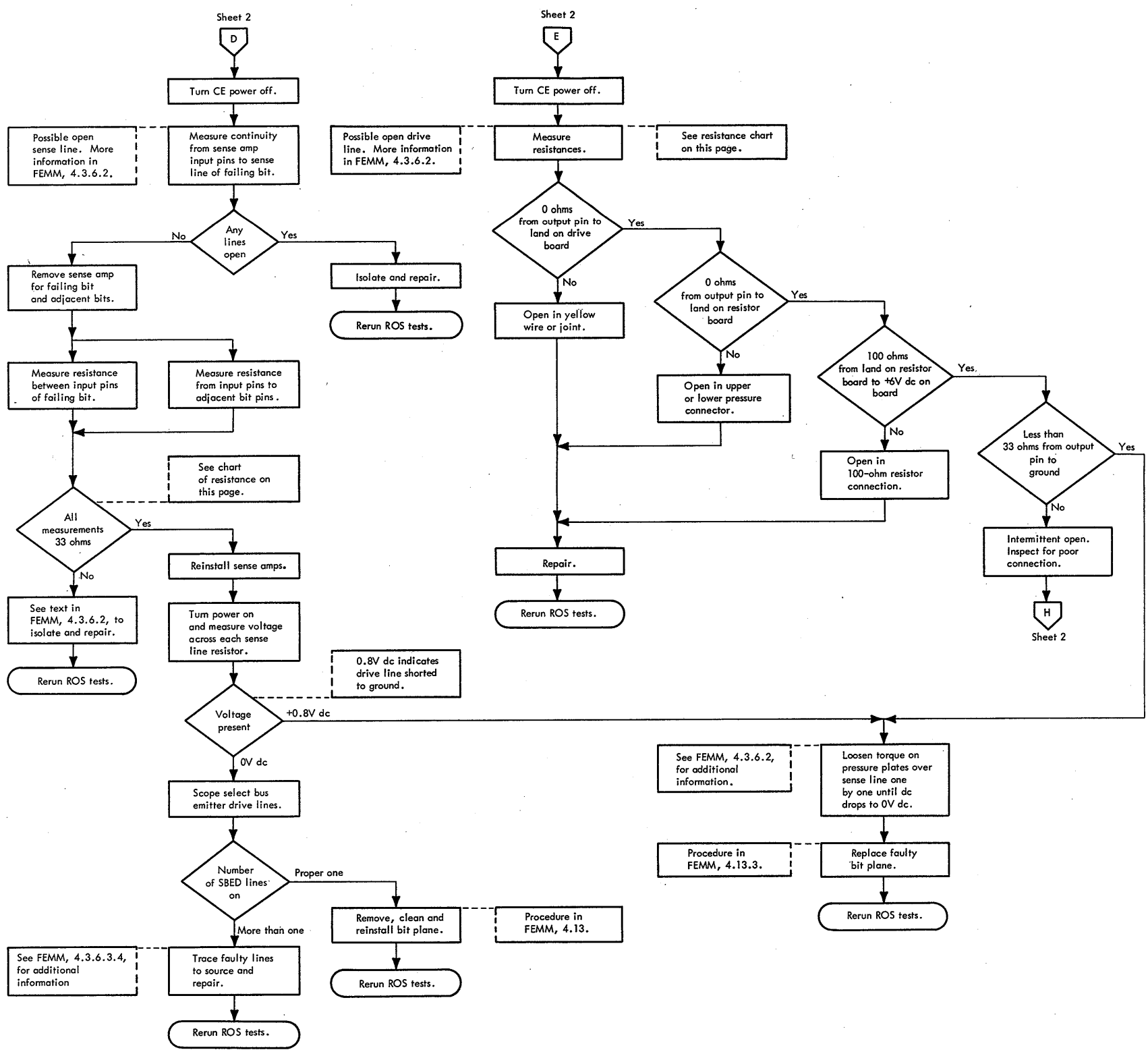


Diagram 1-2. ROS Test Flowchart (Sheet 2 of 3)



Resistance Readings

Condition	From Sense Amp Input to	Resistance
Normal	DC return. Any other sense amp input. Any drive/balance line.	16.5 ohms 33.0 ohms Open
Sense - sense line short	DC return. Input of sense amp to which it is shorted. Any other sense amp input. Any drive/balance line.	8.25 ohms 0 ohm 24.75 ohms Open
Sense - DC return short	DC return. Any other sense amp input. Any drive/balance line.	0 ohm 16.5 ohms Open
Sense - drive/balance line short	DC return. Drive/balance line to which it is shorted. Any drive/balance line in same or opposite plane, except line to which it is shorted. Any drive/balance line not in same or opposite plane.	16.5 ohms 0 ohm 200 ohms plus short resistance Open

Diagram 1-2. ROS Test Flowchart (Sheet 3 of 3)

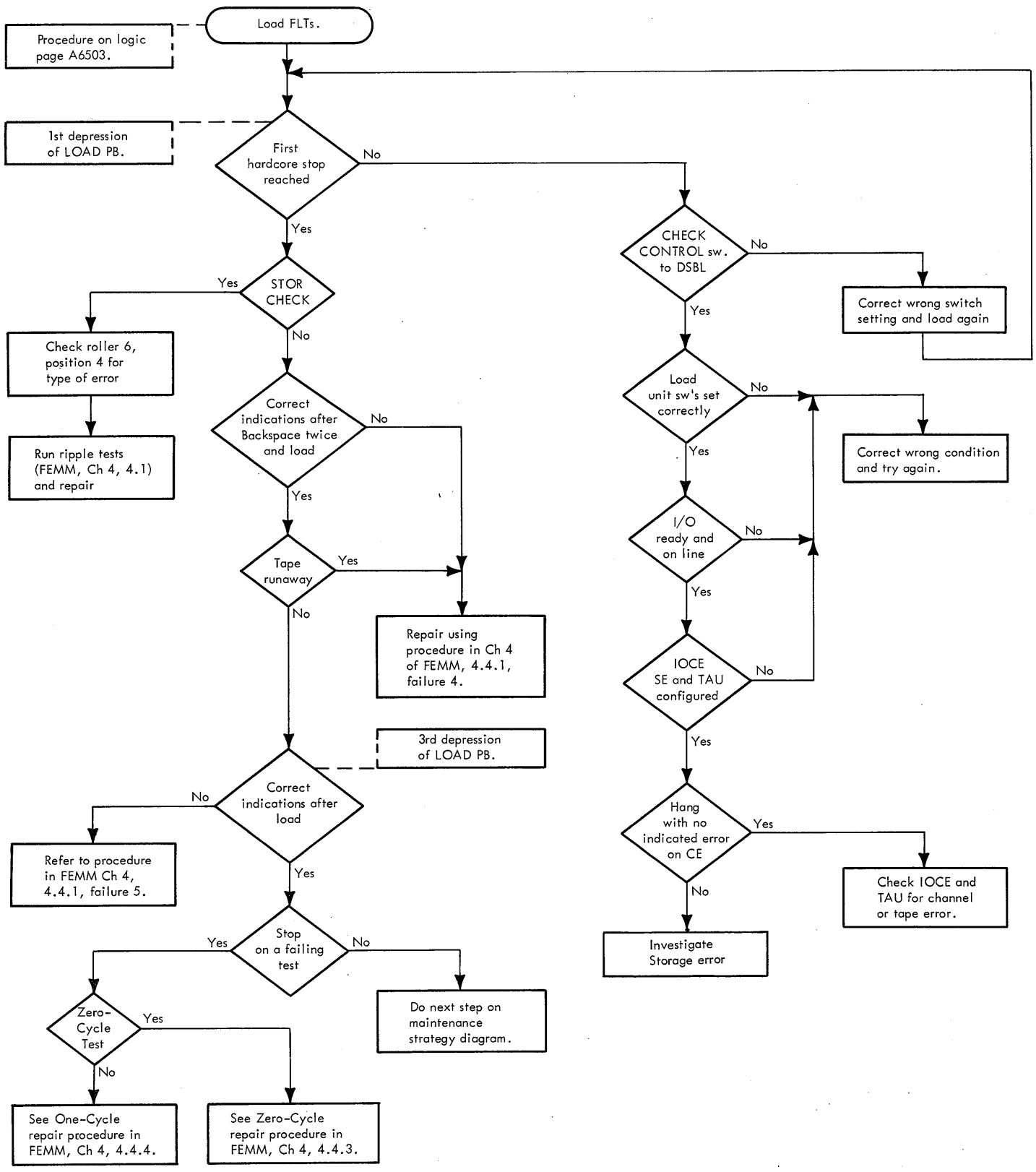


Diagram 1-3. FLT Flowchart

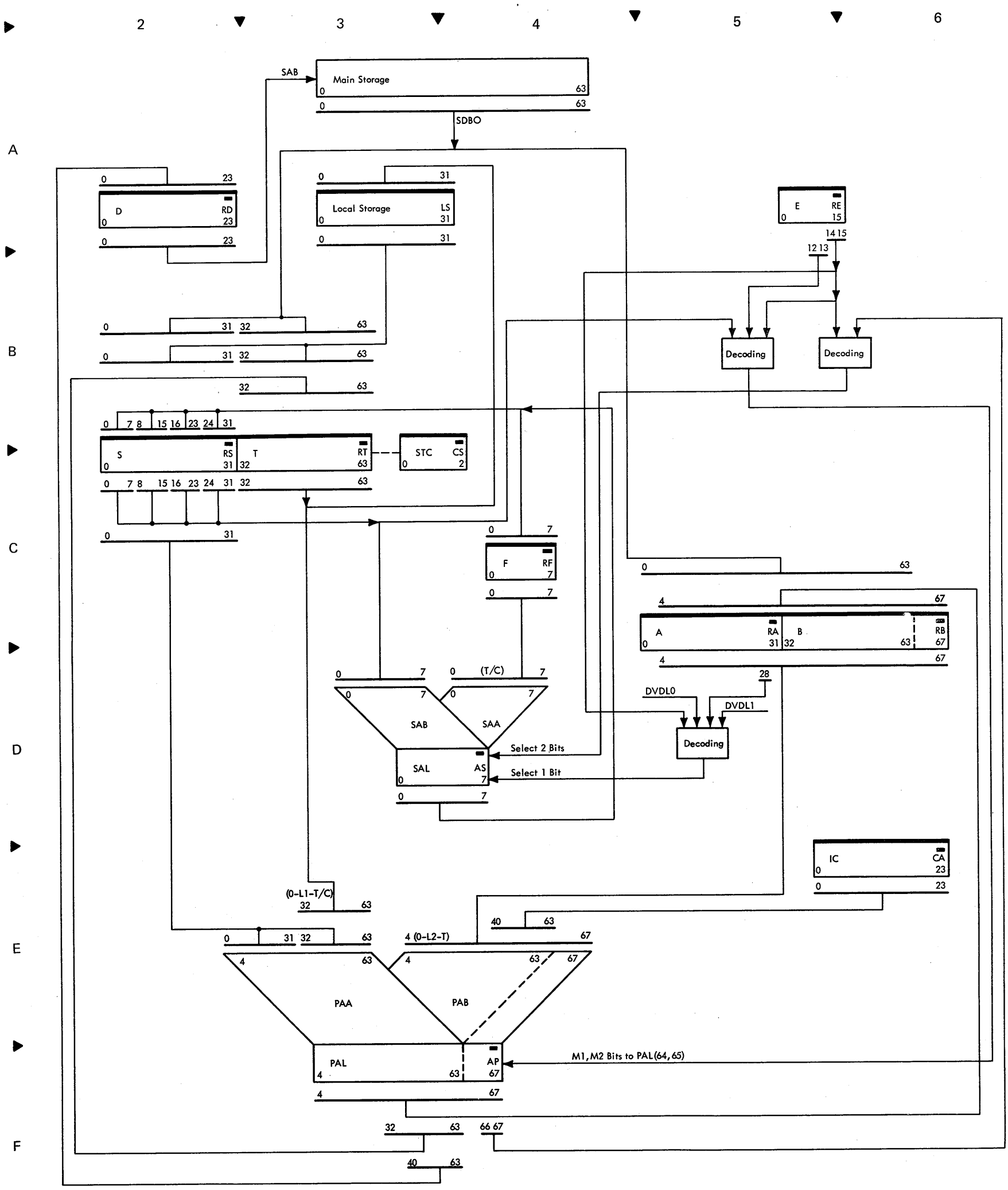


Diagram 3-1. Fixed Point Instruction Data Flow

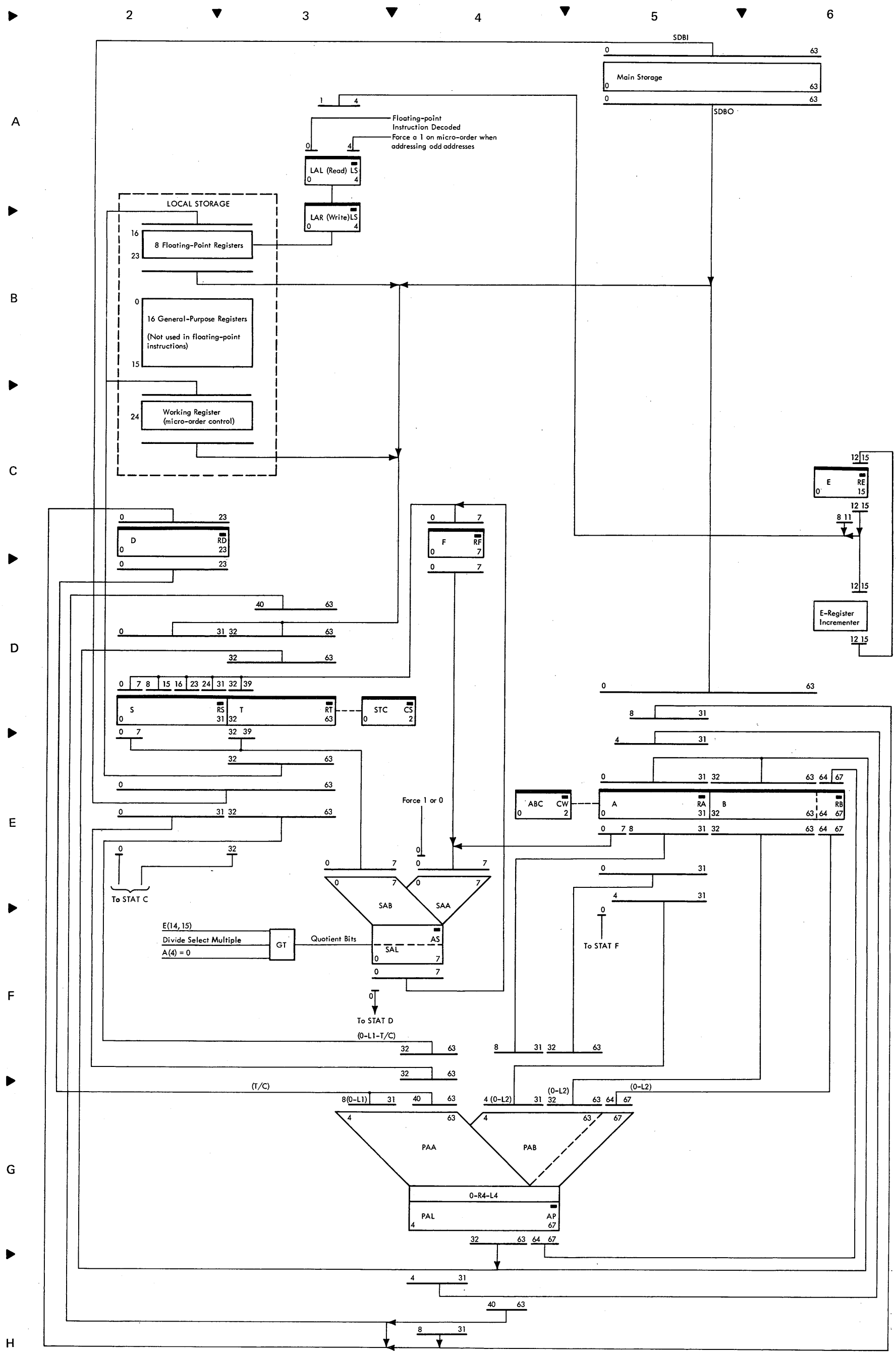


Diagram 3-2. Floating-Point Instruction Data Flow

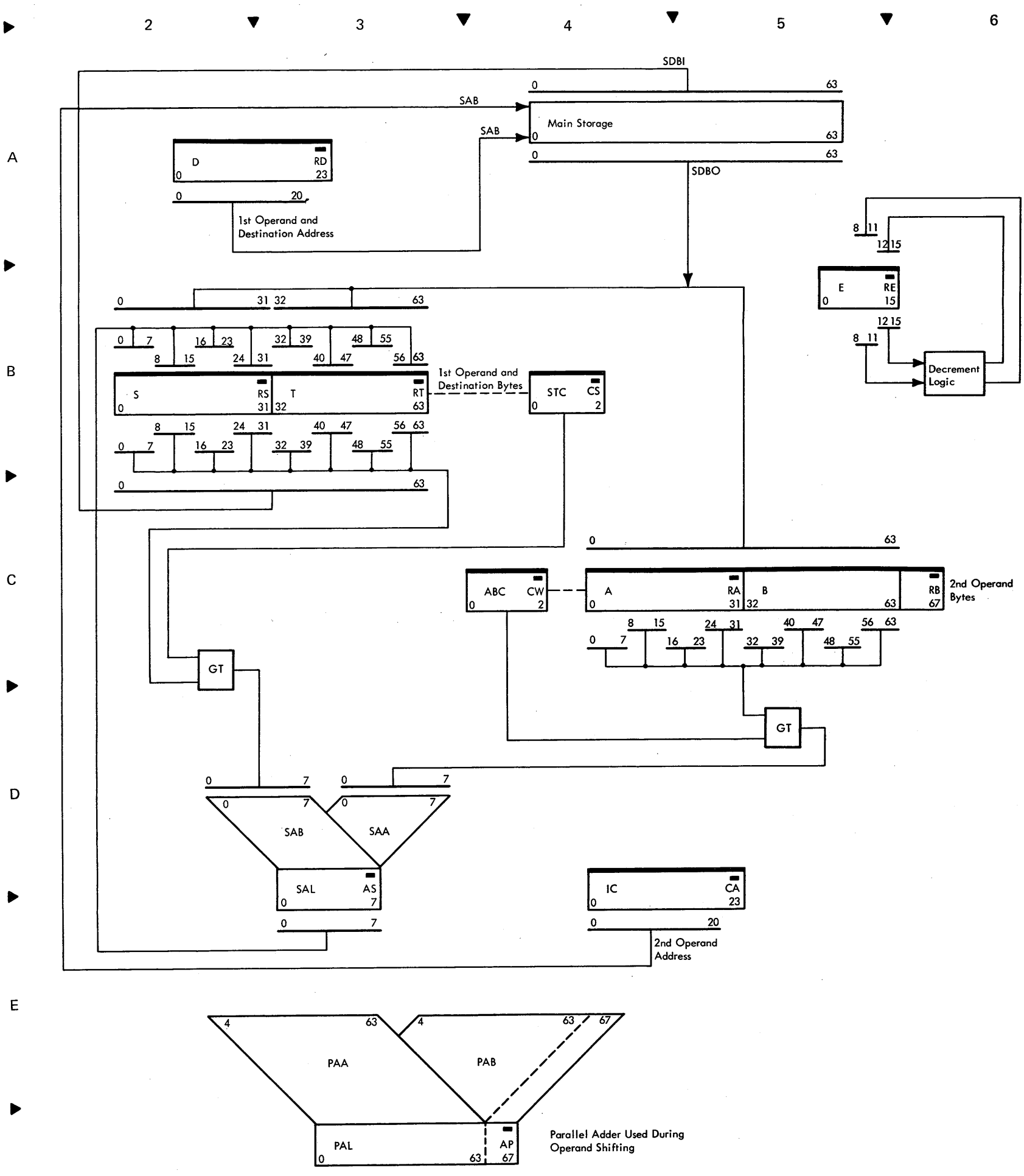


Diagram 3-3. Decimal and Logical Instruction Data Flow

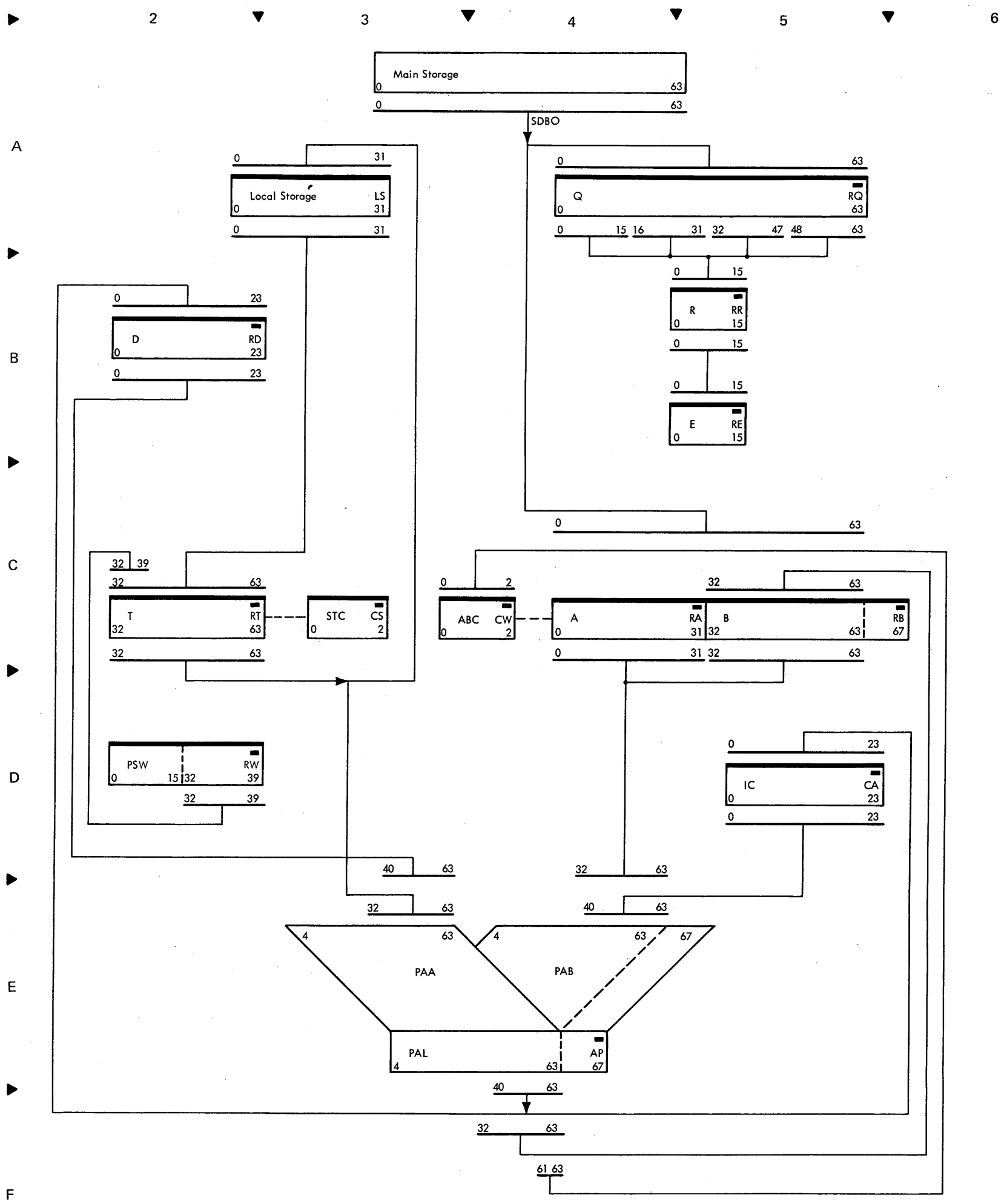


Diagram 3-4. Branching Instruction Data Flow

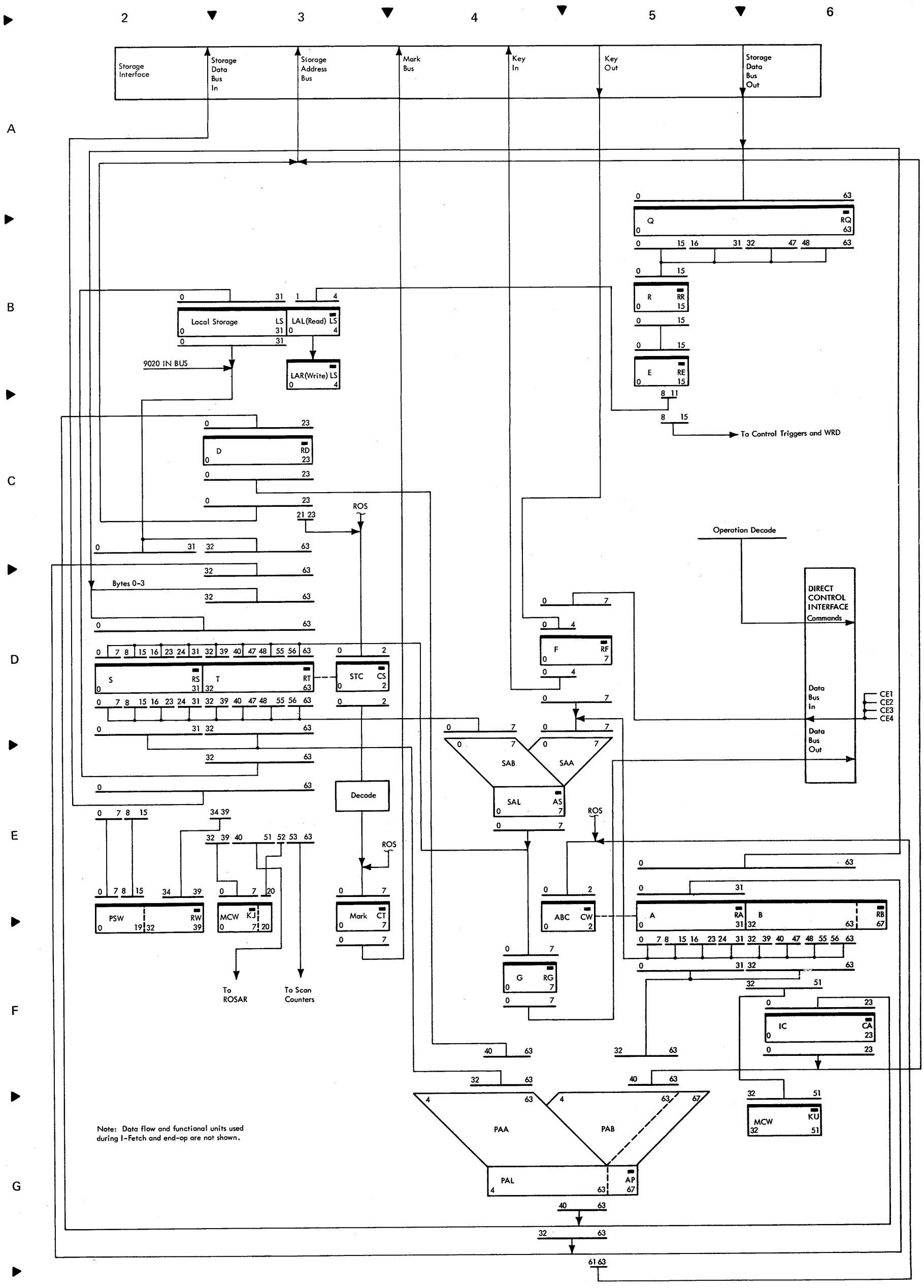


Diagram 3-5. Status Switching Instruction Data Flow

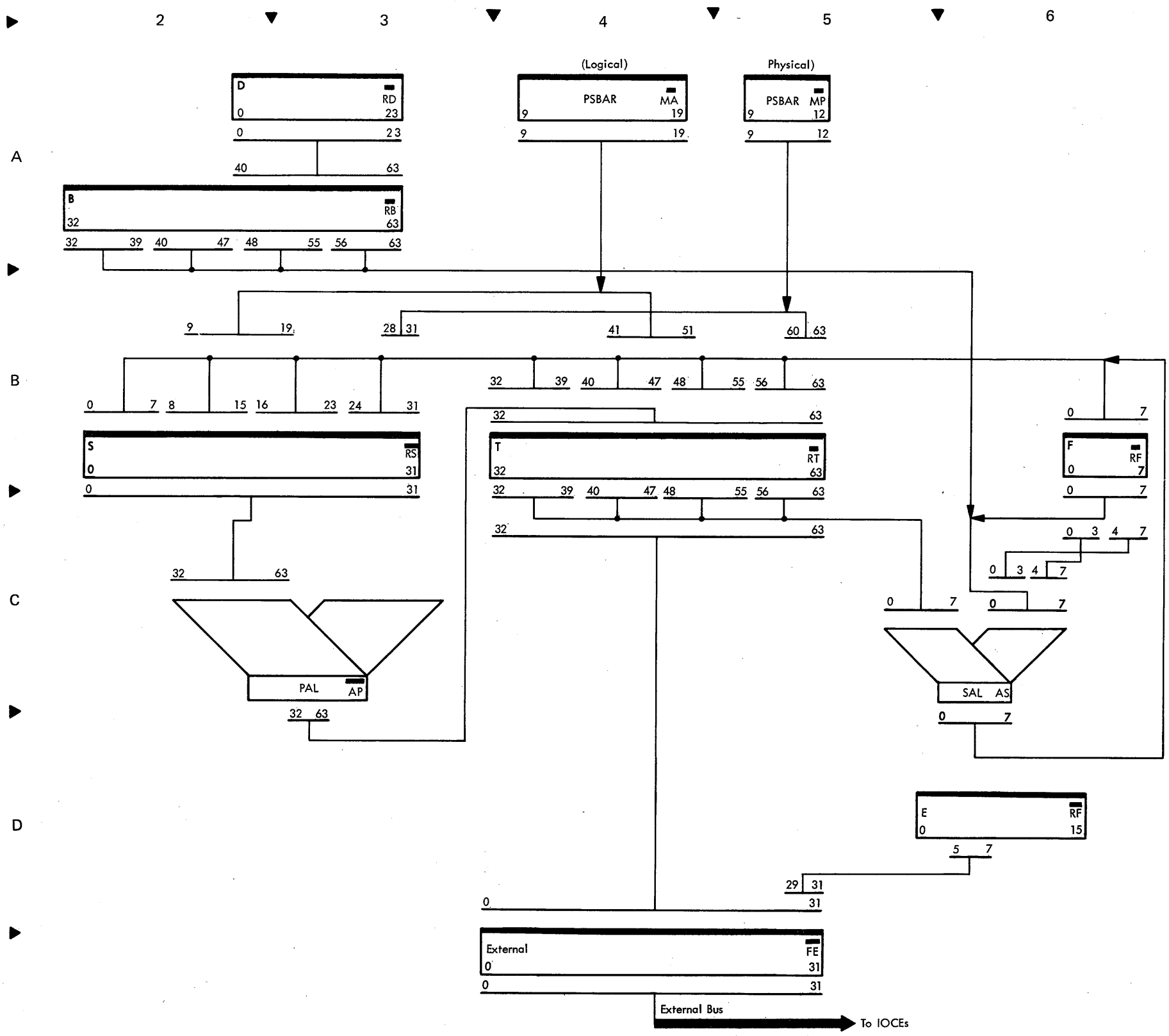


Diagram 3-6. Input/Output Instruction Data Flow

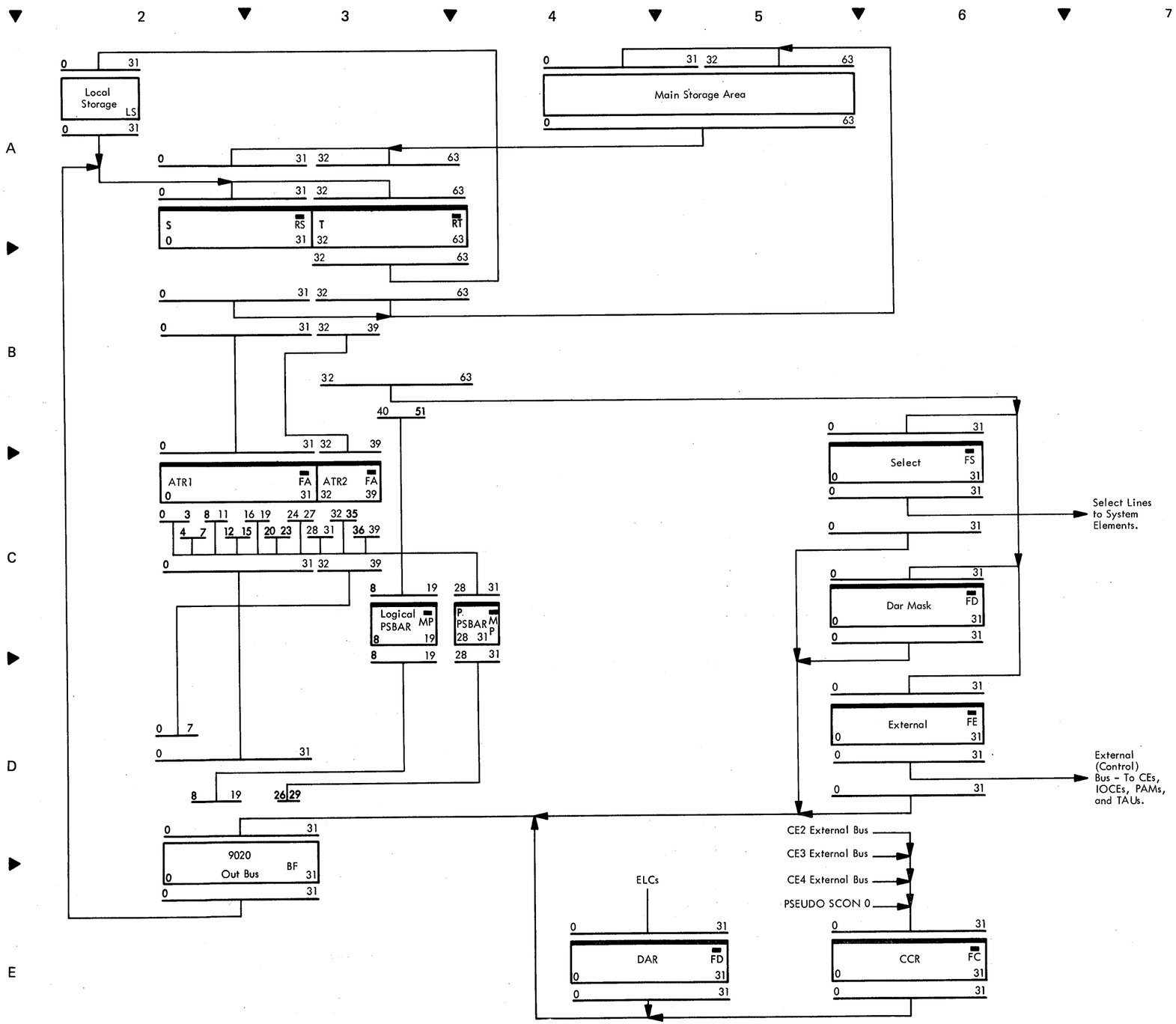


Diagram 3-7. Multiple Computing Element Instruction Data Flow

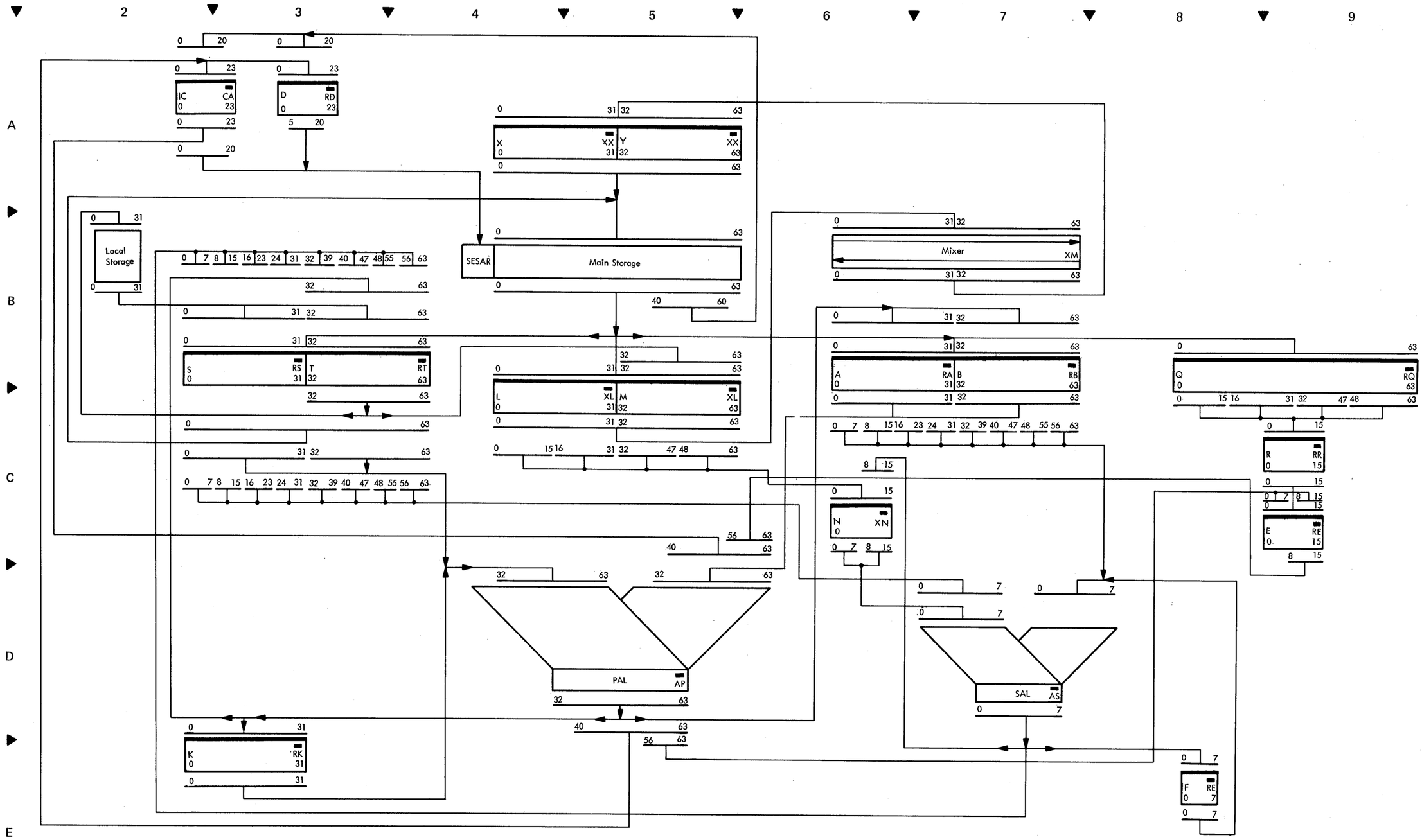
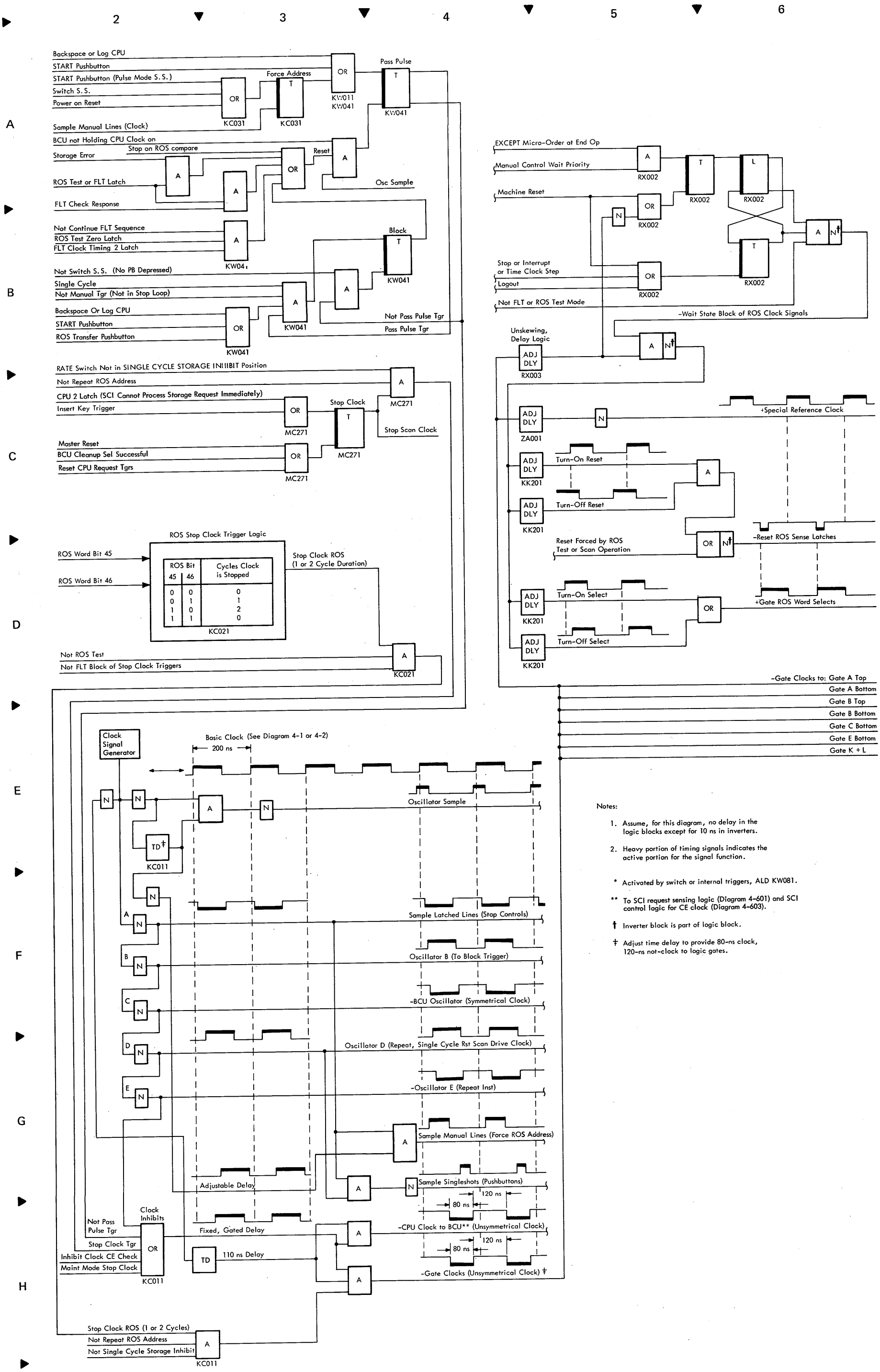


Diagram 3-8. Display Instruction Data Flow



Notes:

1. Assume, for this diagram, no delay in the logic blocks except for 10 ns in inverters.
2. Heavy portion of timing signals indicates the active portion for the signal function.

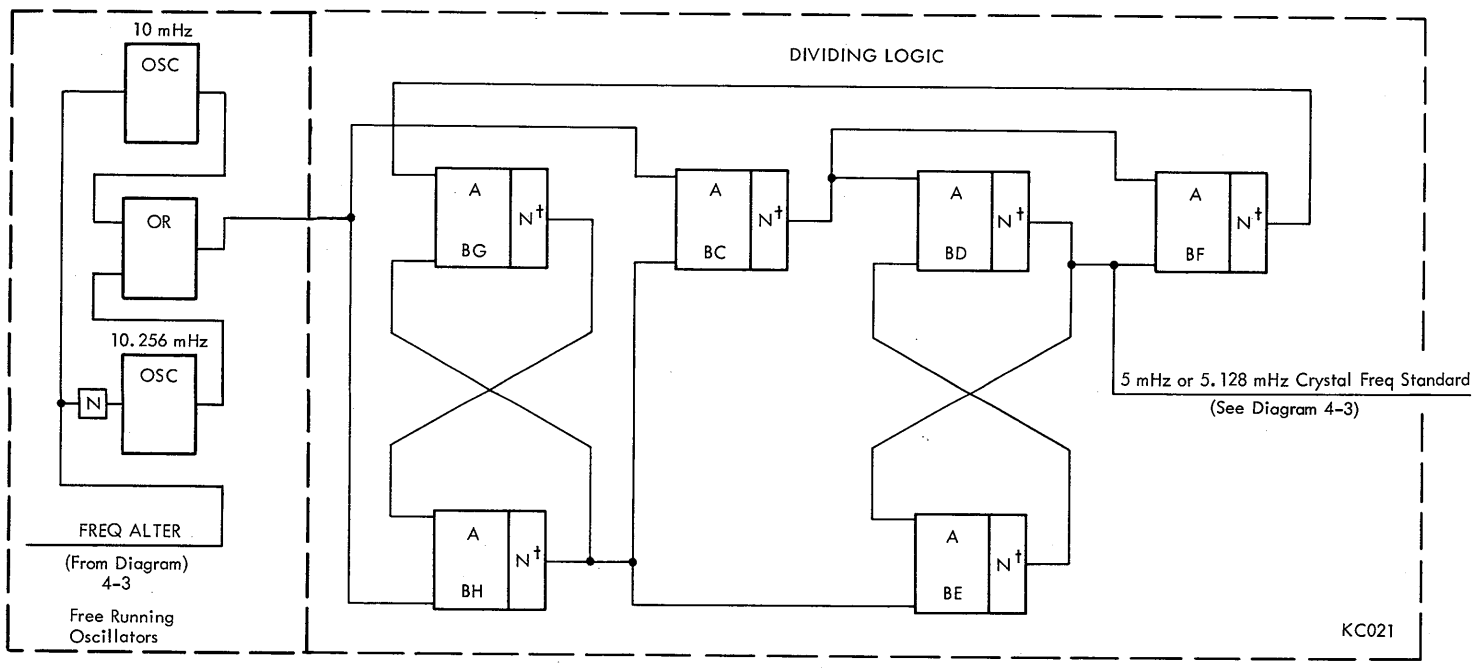
* Activated by switch or internal triggers, ALD KW081.

** To SCI request sensing logic (Diagram 4-601) and SCI control logic for CE clock (Diagram 4-603).

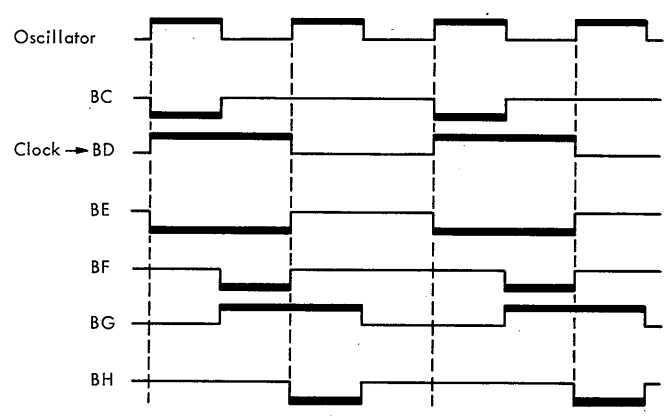
† Inverter block is part of logic block.

‡ Adjust time delay to provide 80-ns clock, 120-ns not-clock to logic gates.

Diagram 4-1. Clock Control Logic



Ideal Waveform At Output Of Each AND After Inversion:



Notes:

1. Heavy portion of timing signals indicates the active portion for the signal function.
2. The two letter notation within the AND's is the block serial number on ALD KC021.

†Inverter block is part of logic block.

Diagram 4-2. Reference Oscillator

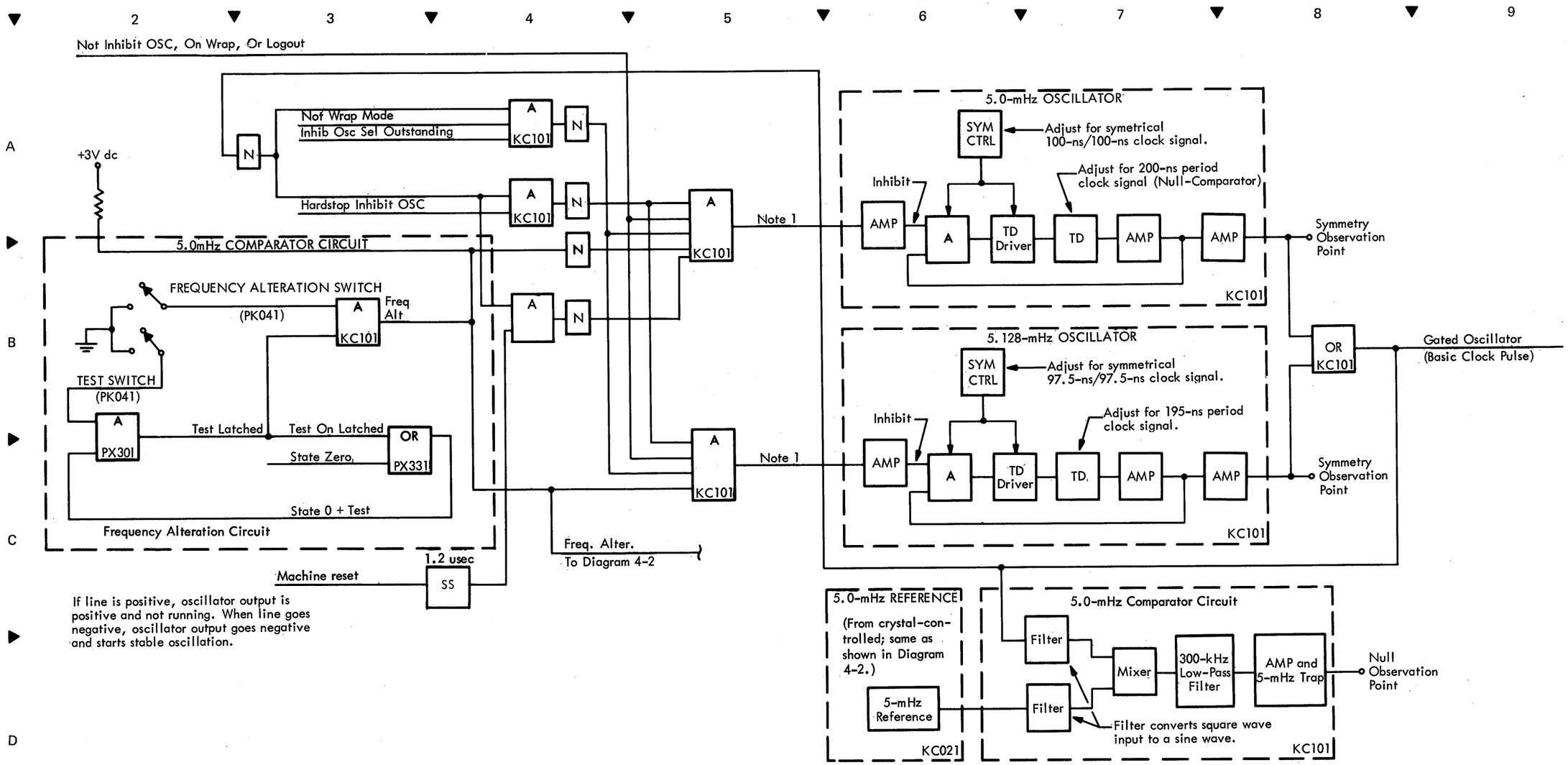


Diagram 4-3. CE Clock Signal Generator

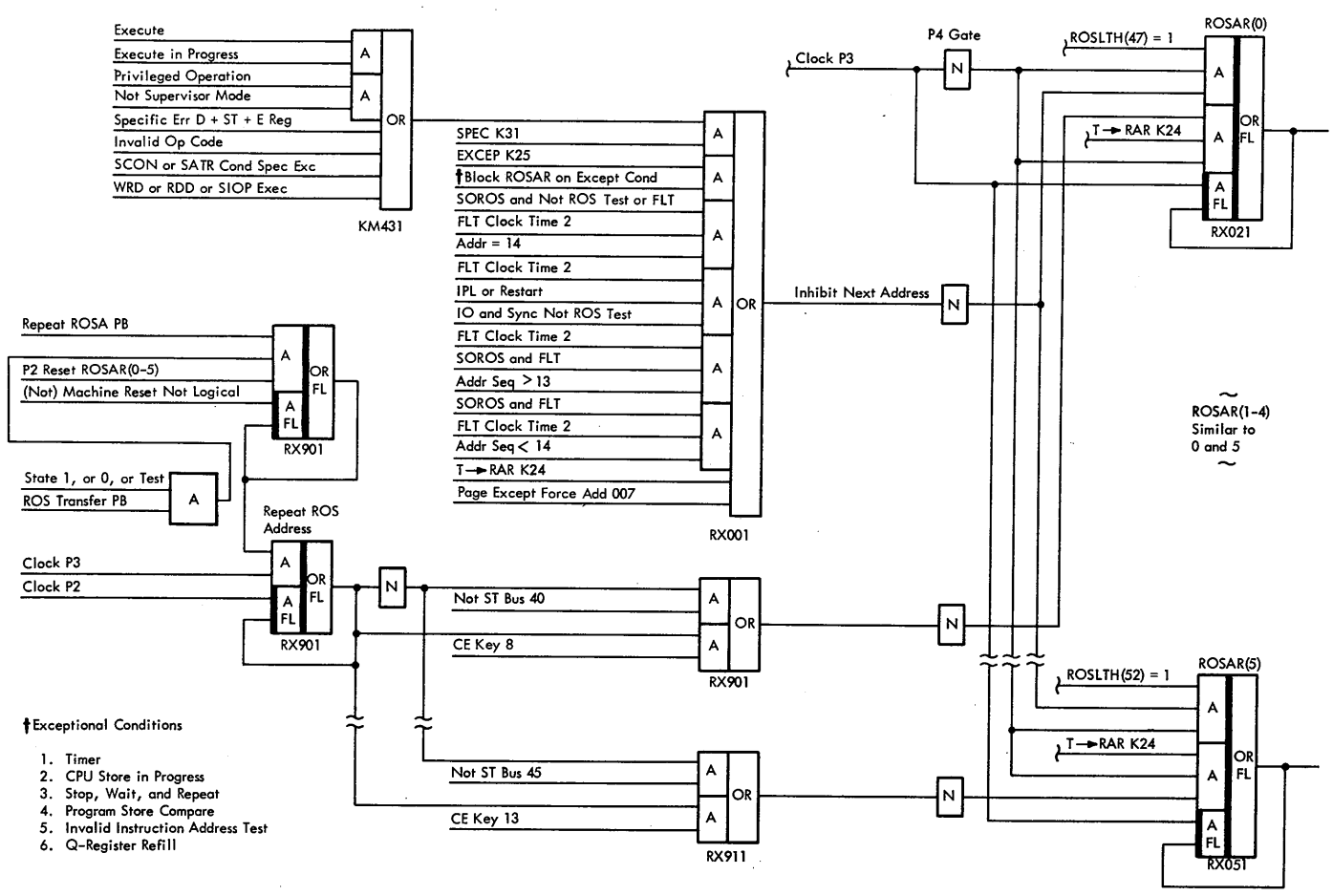


Diagram 4-101. ROSAR (0-5) Logic

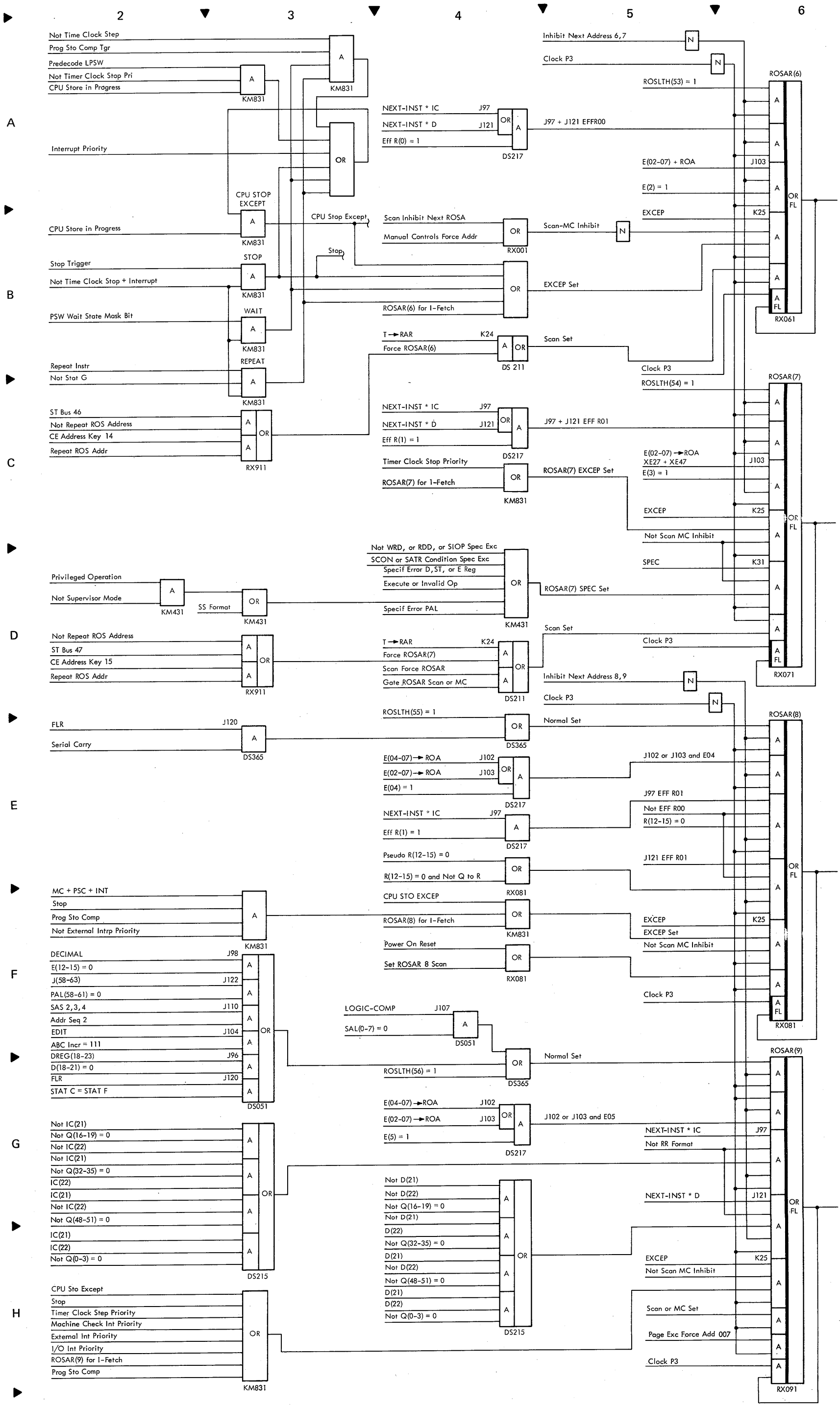


Diagram 4-102. ROSAR (6-9) Logic

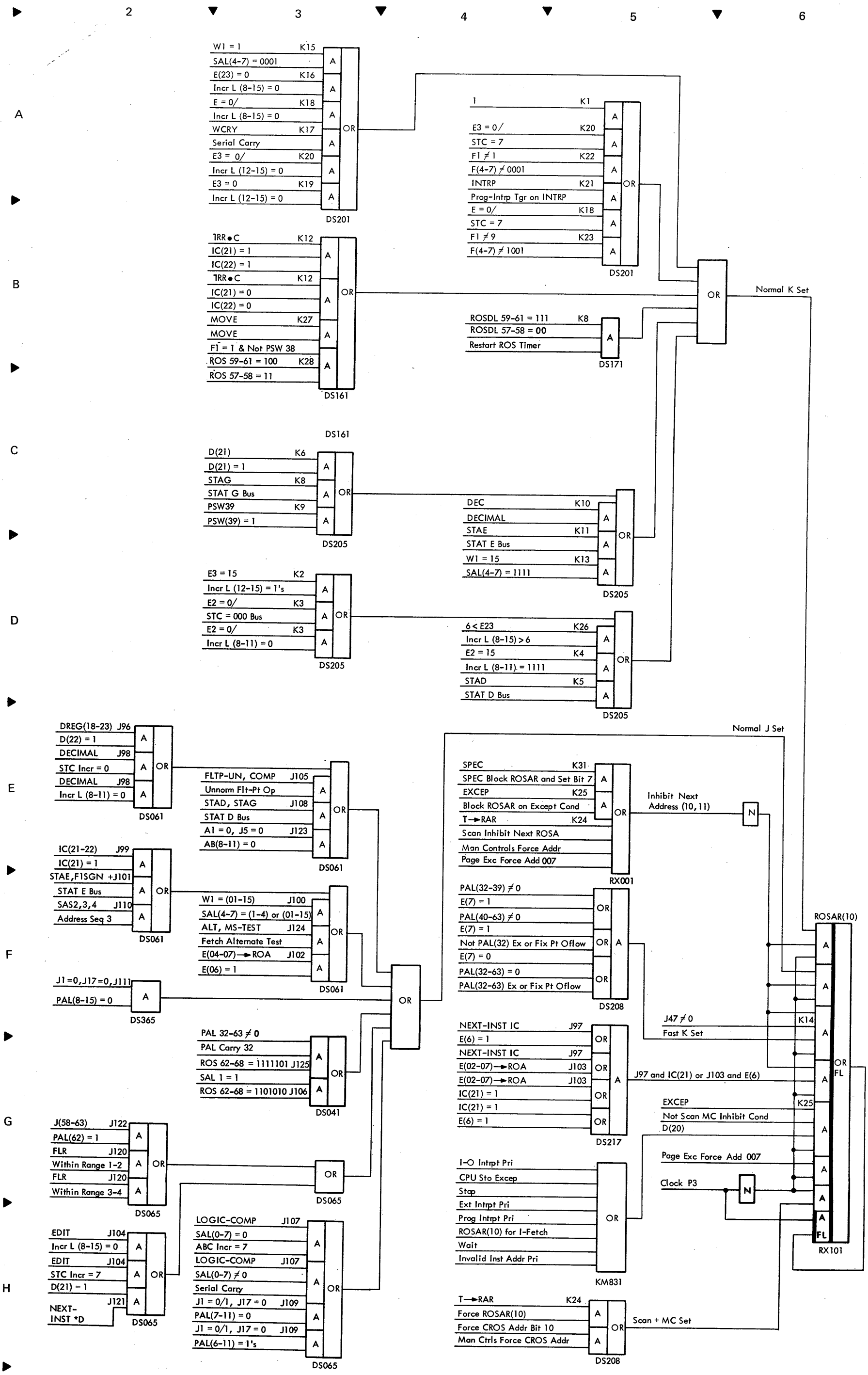


Diagram 4-103. ROSAR (10) Logic

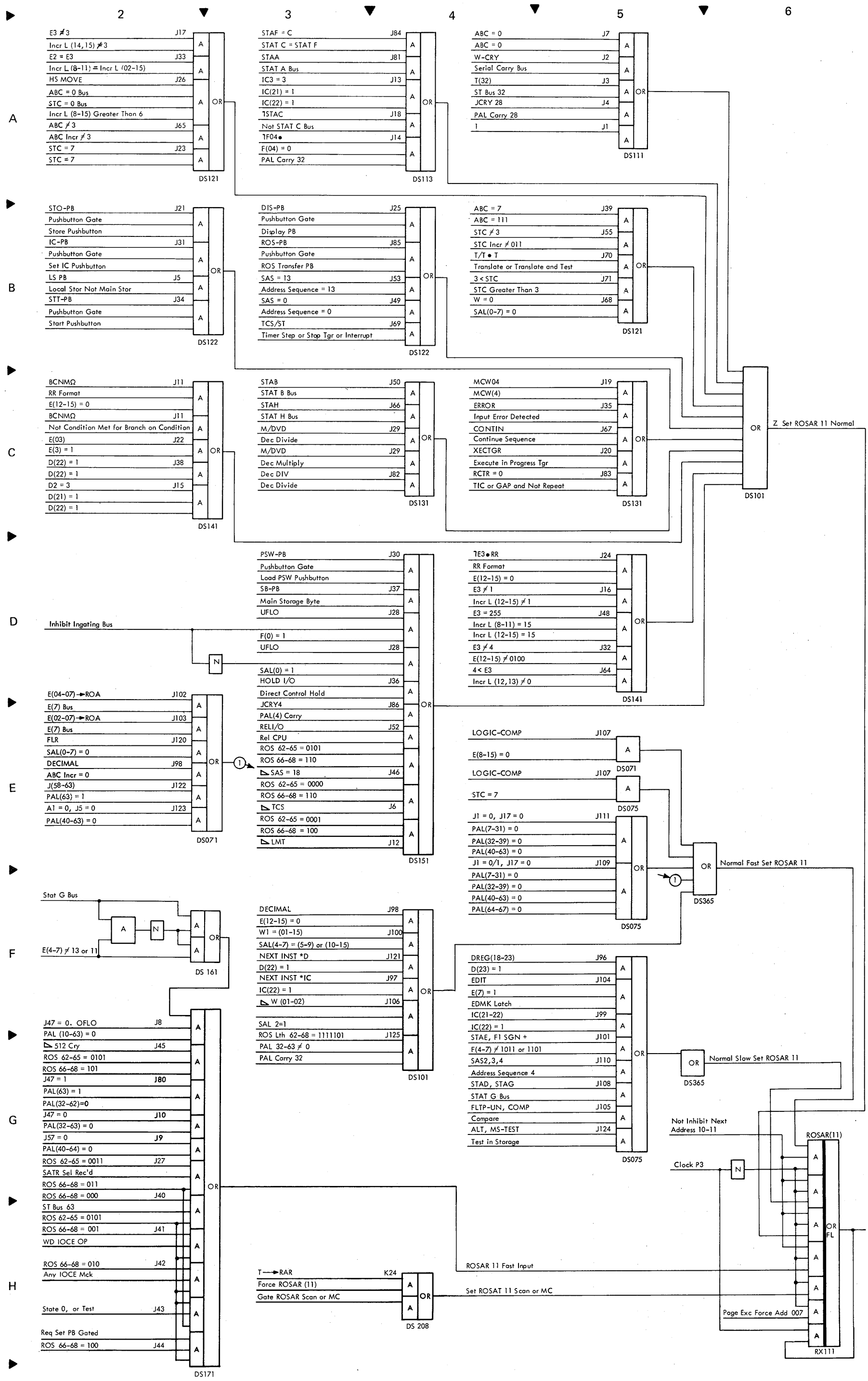


Diagram 4-104. ROSAR (11) Logic

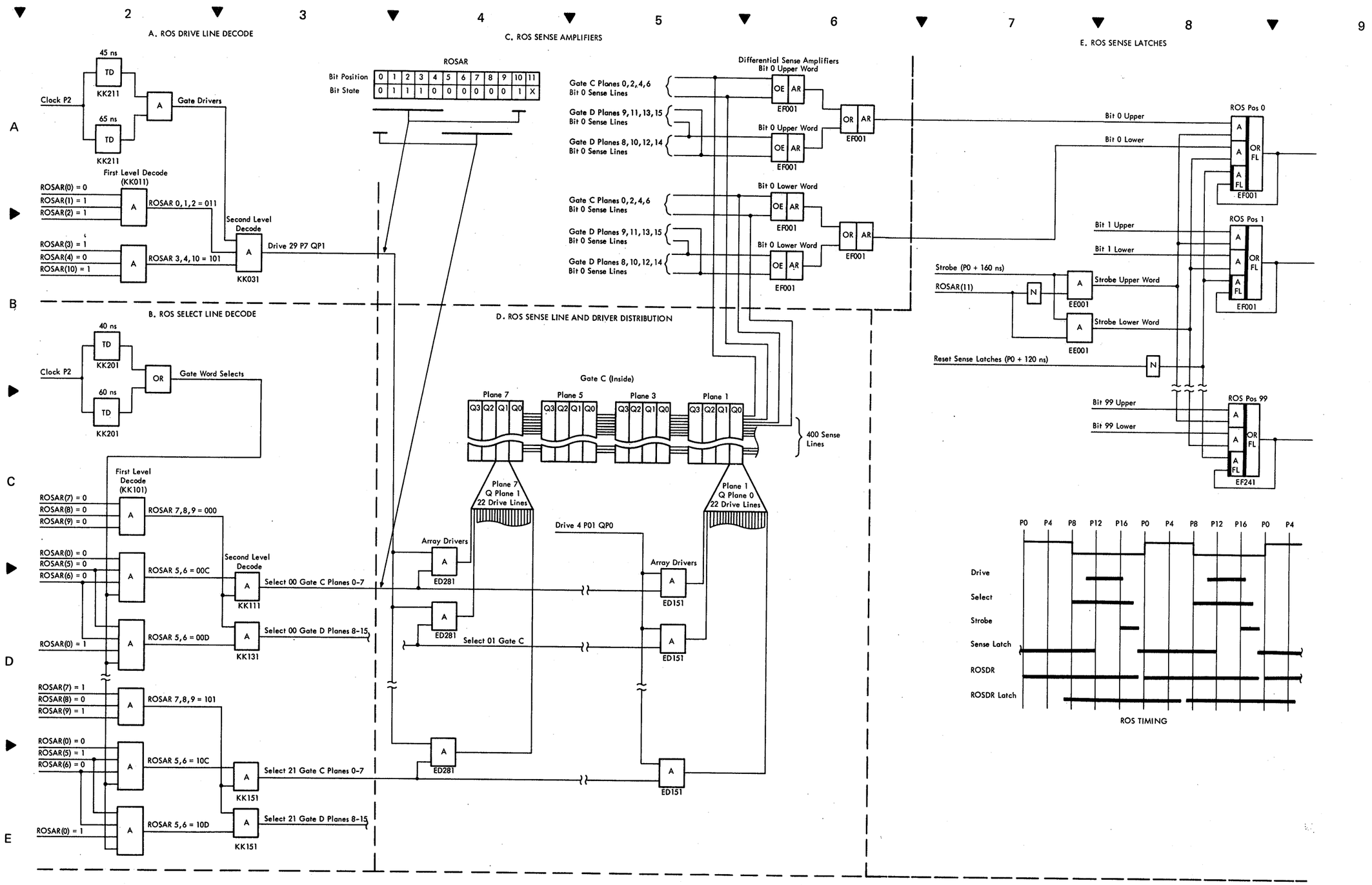
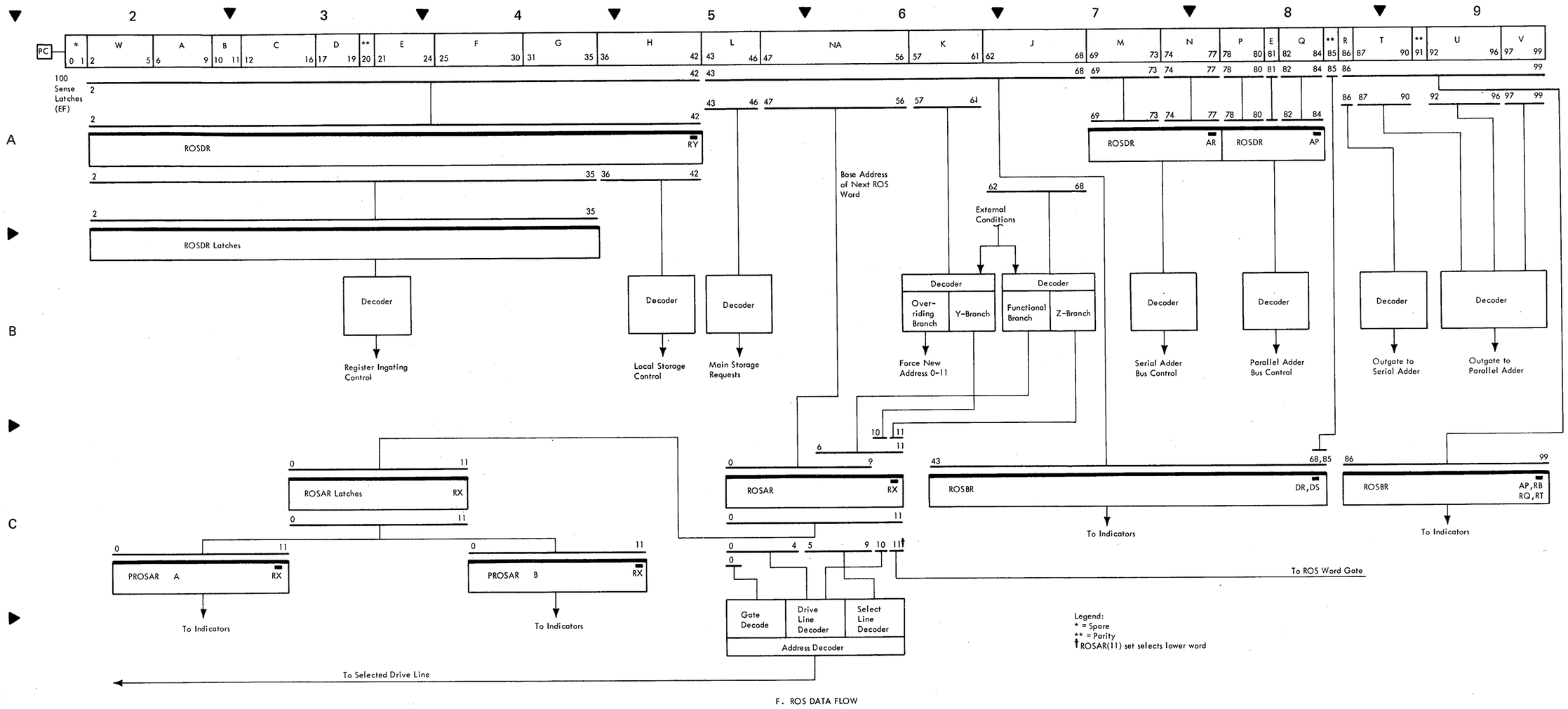


Diagram 4-105. ROS Addressing and Data Flow (Sheet 1 of 2)



F. ROS DATA FLOW

Diagram 4-105. ROS Addressing and Data Flow (Sheet 2 of 2)

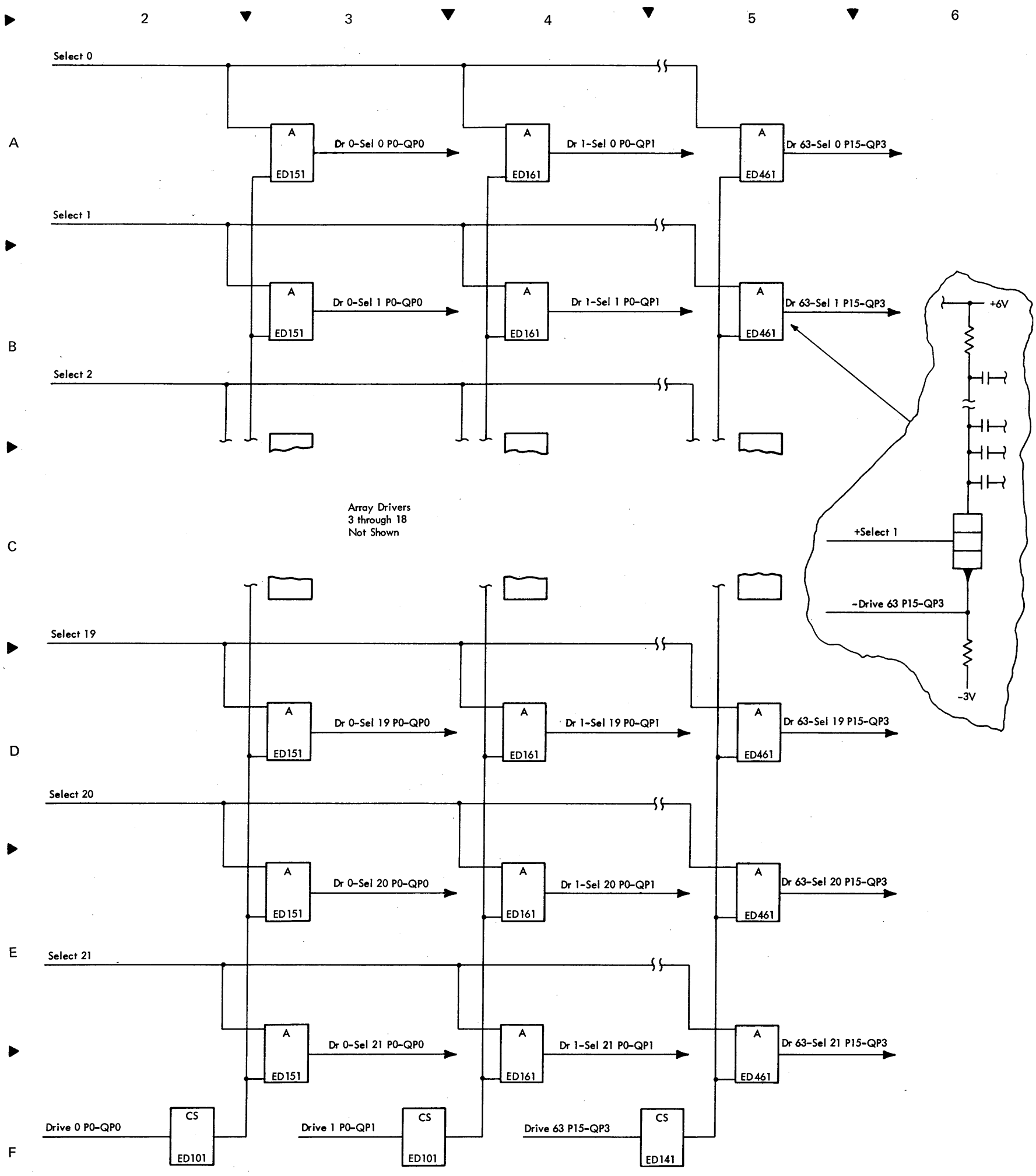
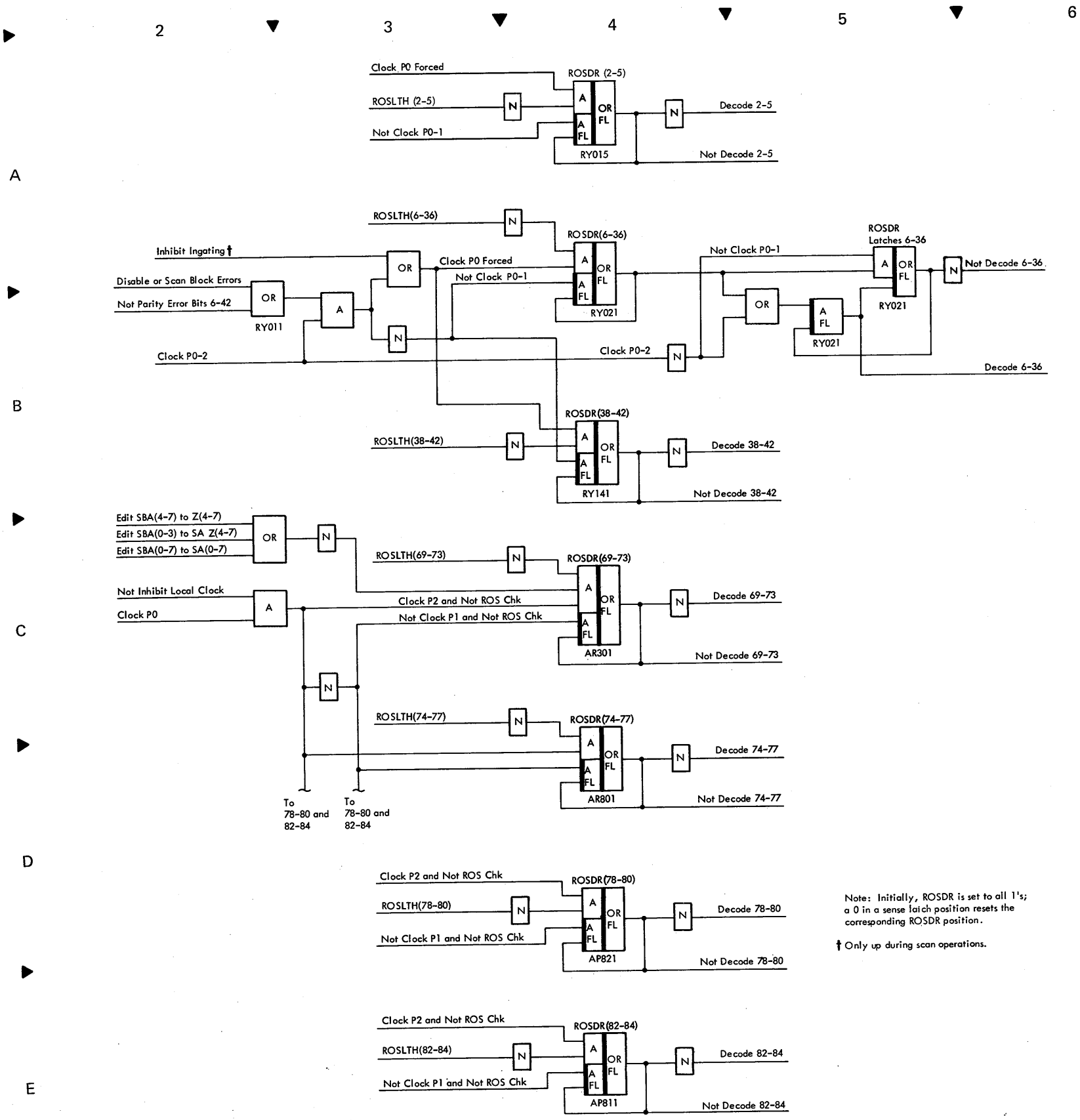


Diagram 4-106. Array Drivers



Note: Initially, ROSDR is set to all 1's; a 0 in a sense latch position resets the corresponding ROSDR position.

† Only up during scan operations.

Diagram 4-107. ROS Data Register

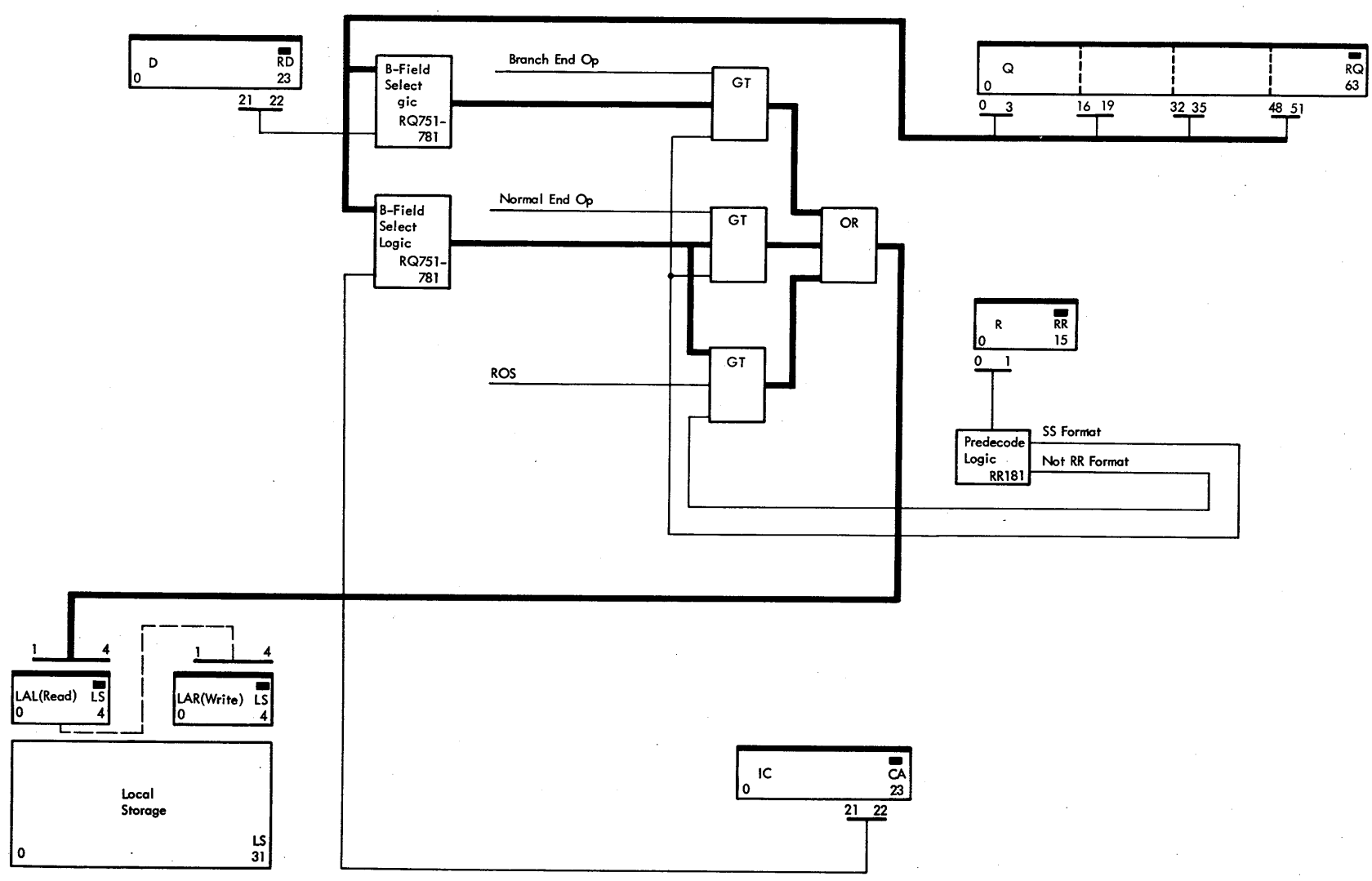


Diagram 4-201. Q-Register B-Field Transfer Controls

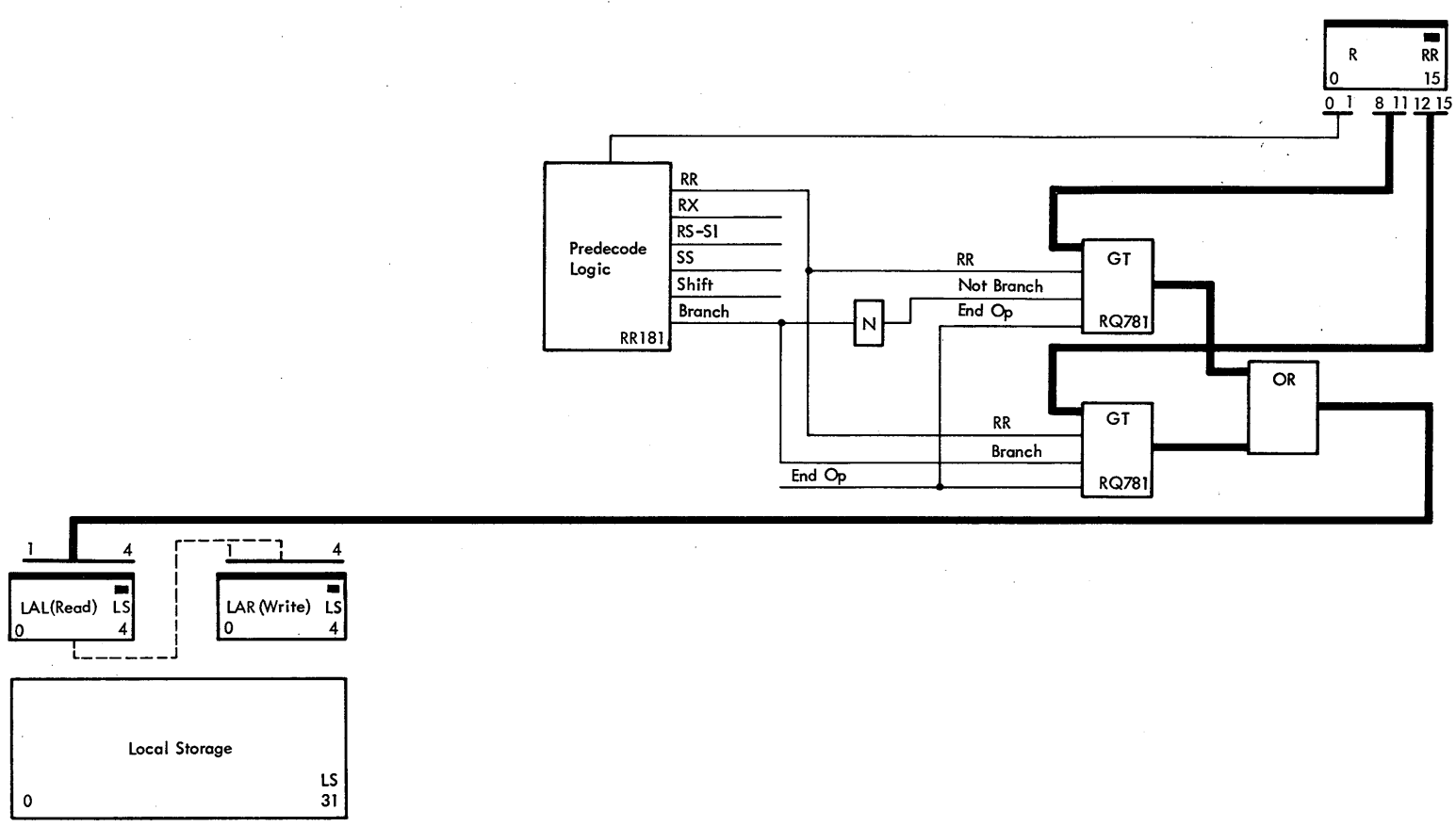


Diagram 4-202. R-Register Transfer to LAL

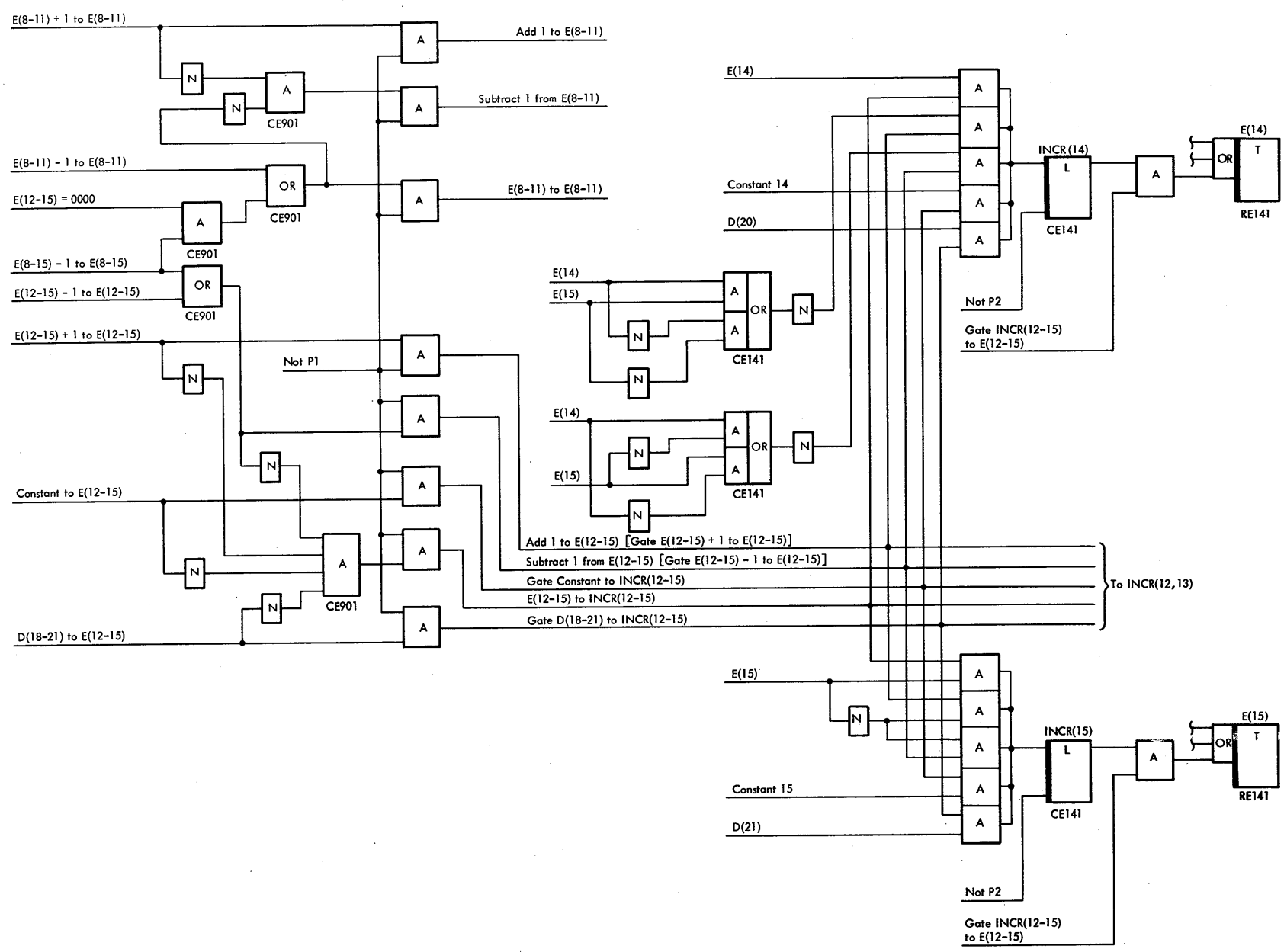


Diagram 4-203. E-Register Incrementer, Bits 14 and 15

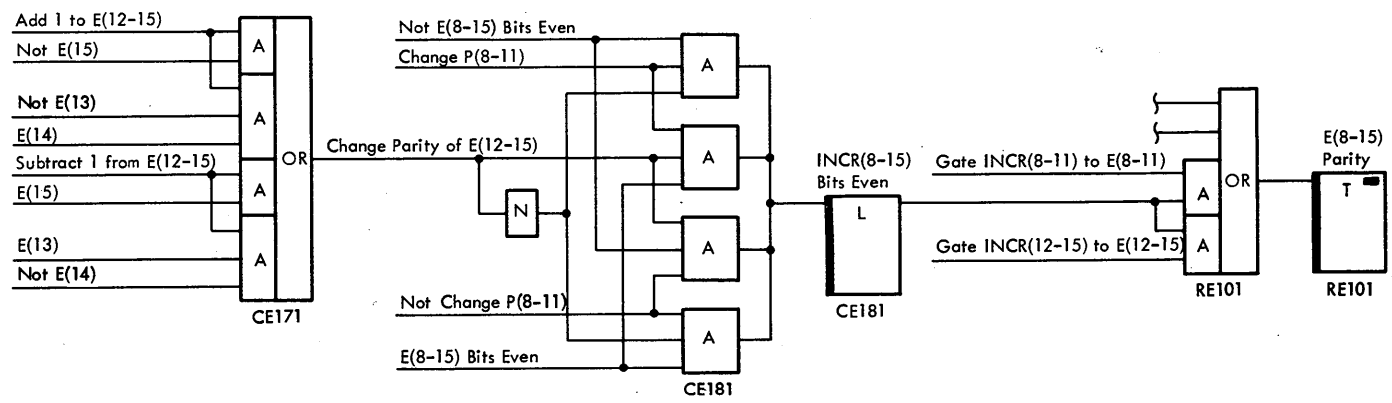


Diagram 4-204. E-Register Parity Prediction after Incrementing

B

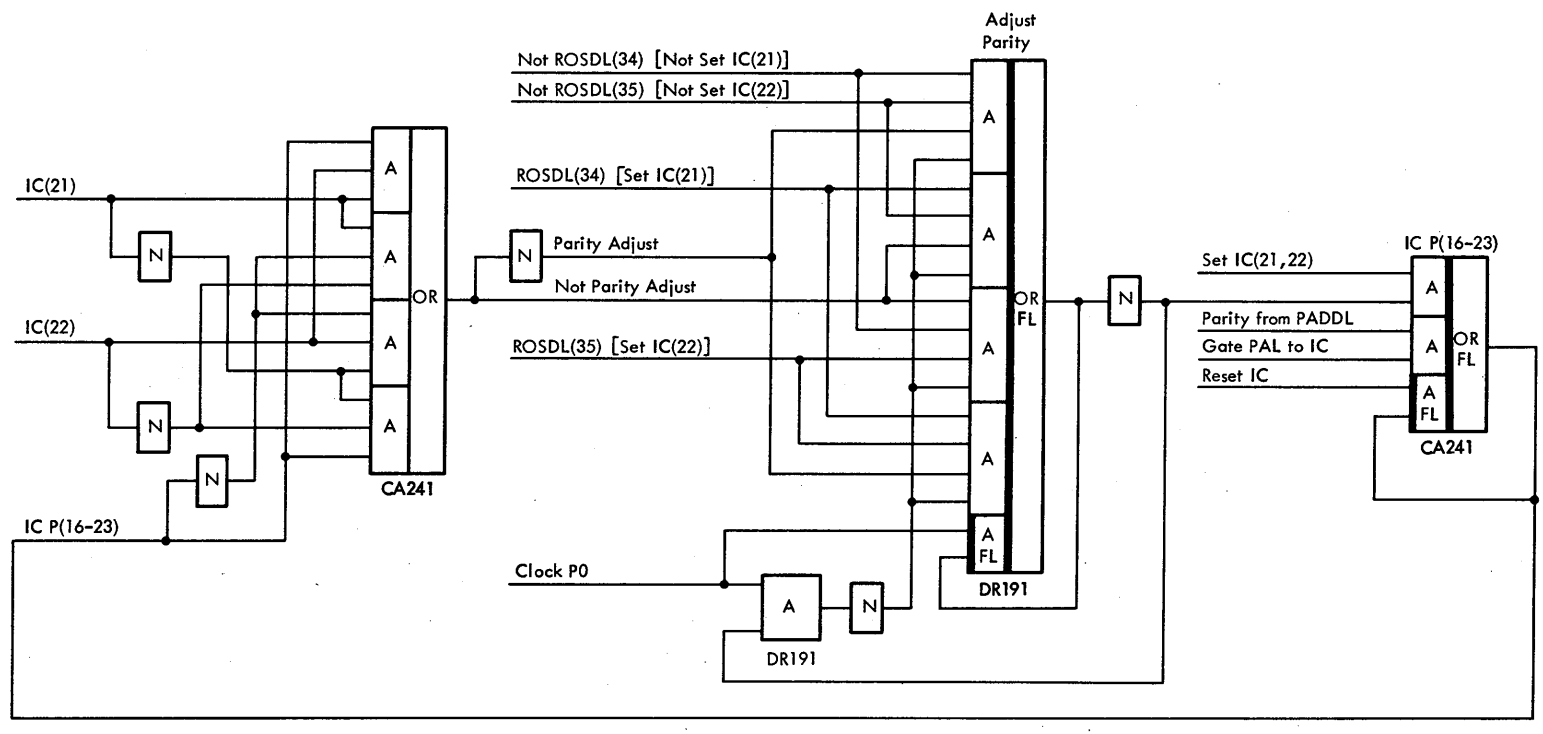


Diagram 4-205. Parity Adjustment for IC (21, 22) Stepping

E

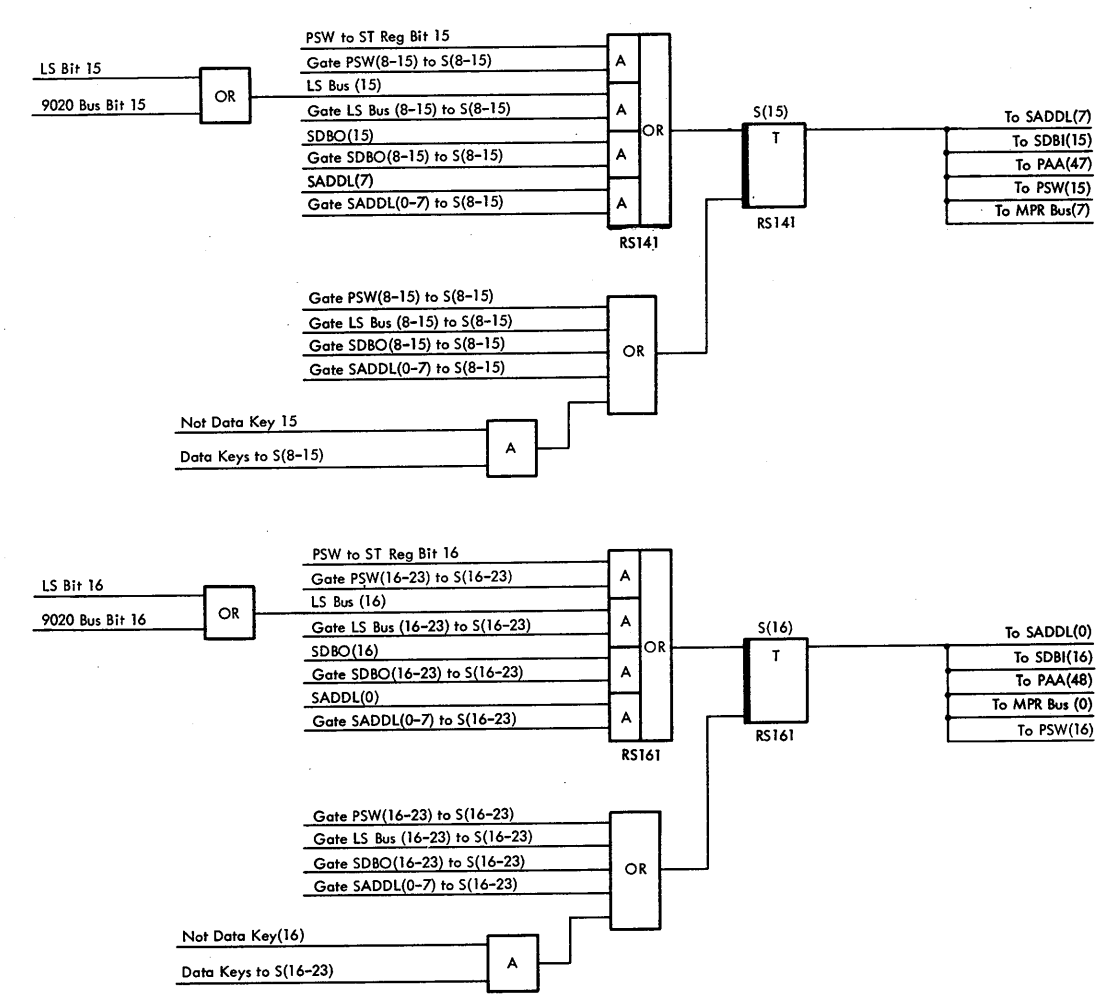


Diagram 4-206. S-Register, Bits 15 and 16

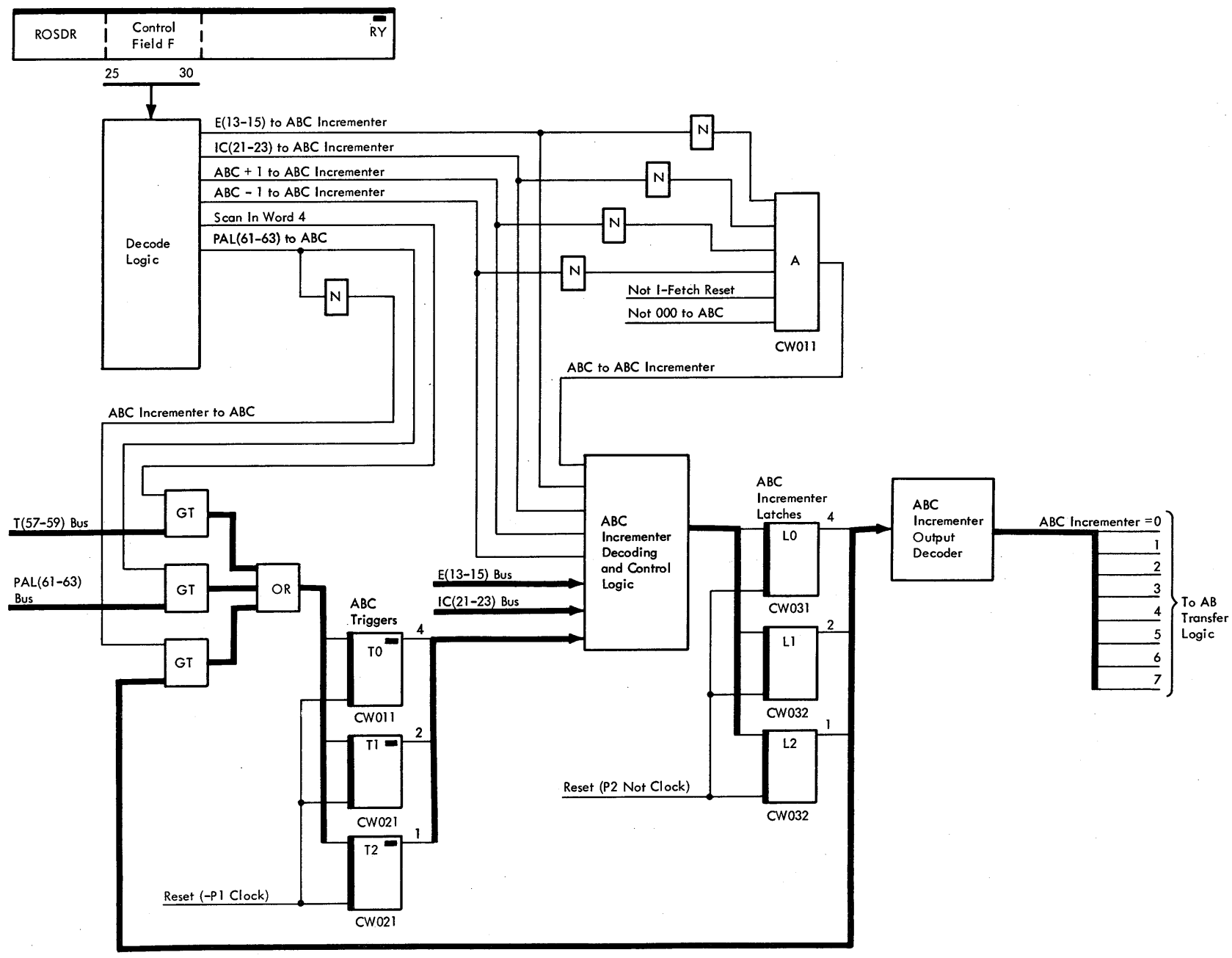


Diagram 4-207. AB Byte Counter

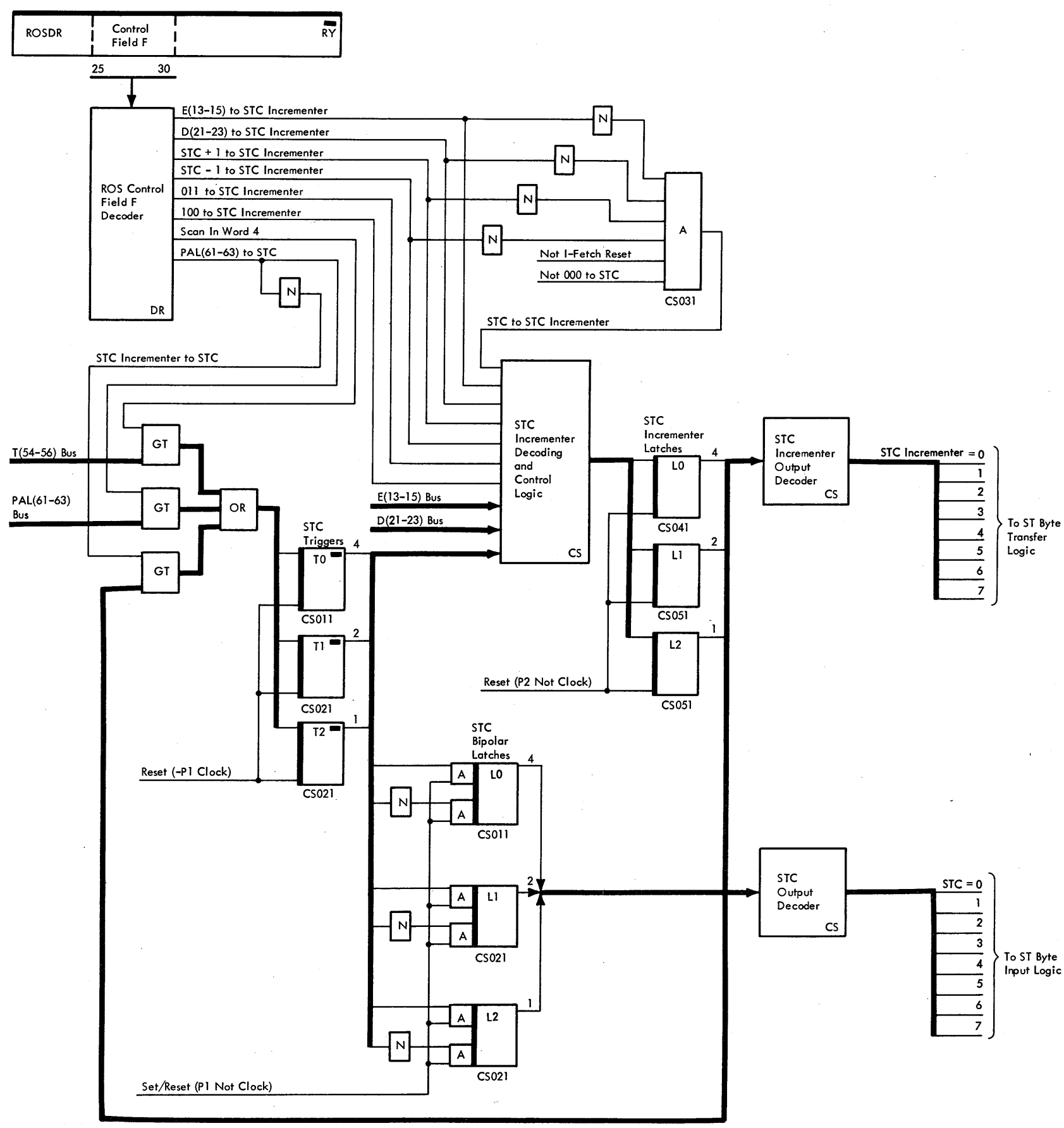


Diagram 4-208. ST Byte Counter

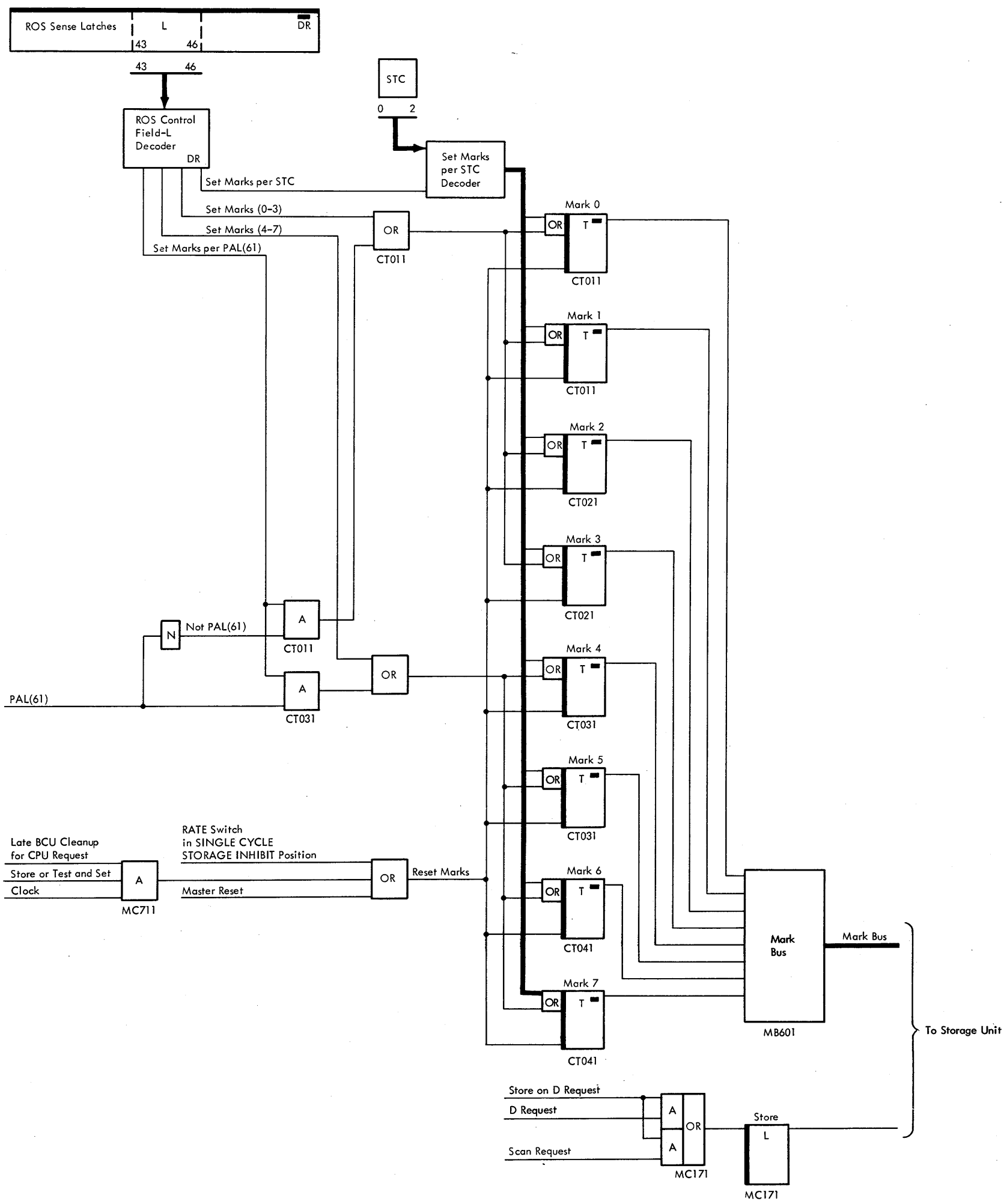


Diagram 4-209. Mark Trigger Logic

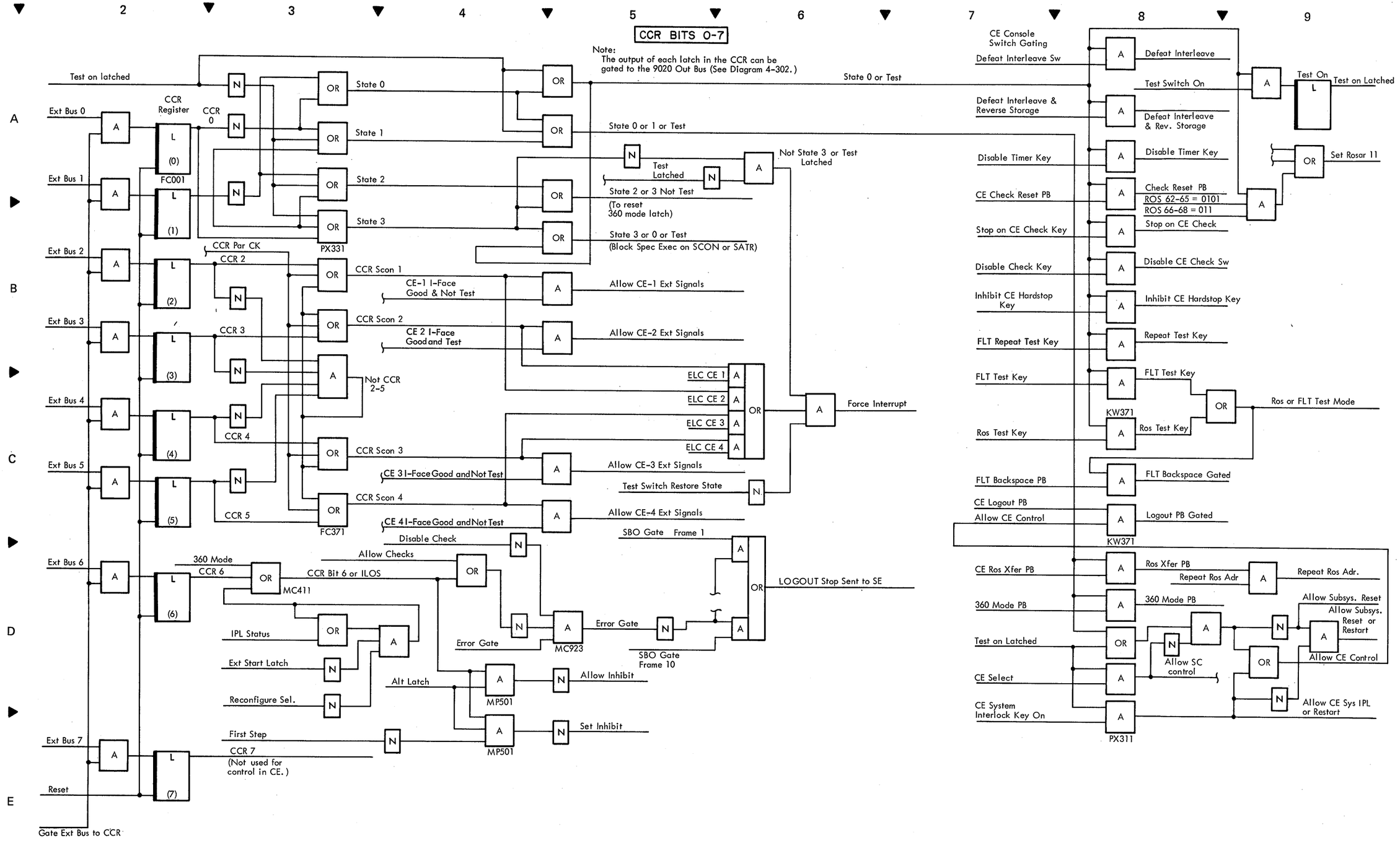


Diagram 4-210. CCR Output Logic and Control Paths (Sheet 1 of 3)

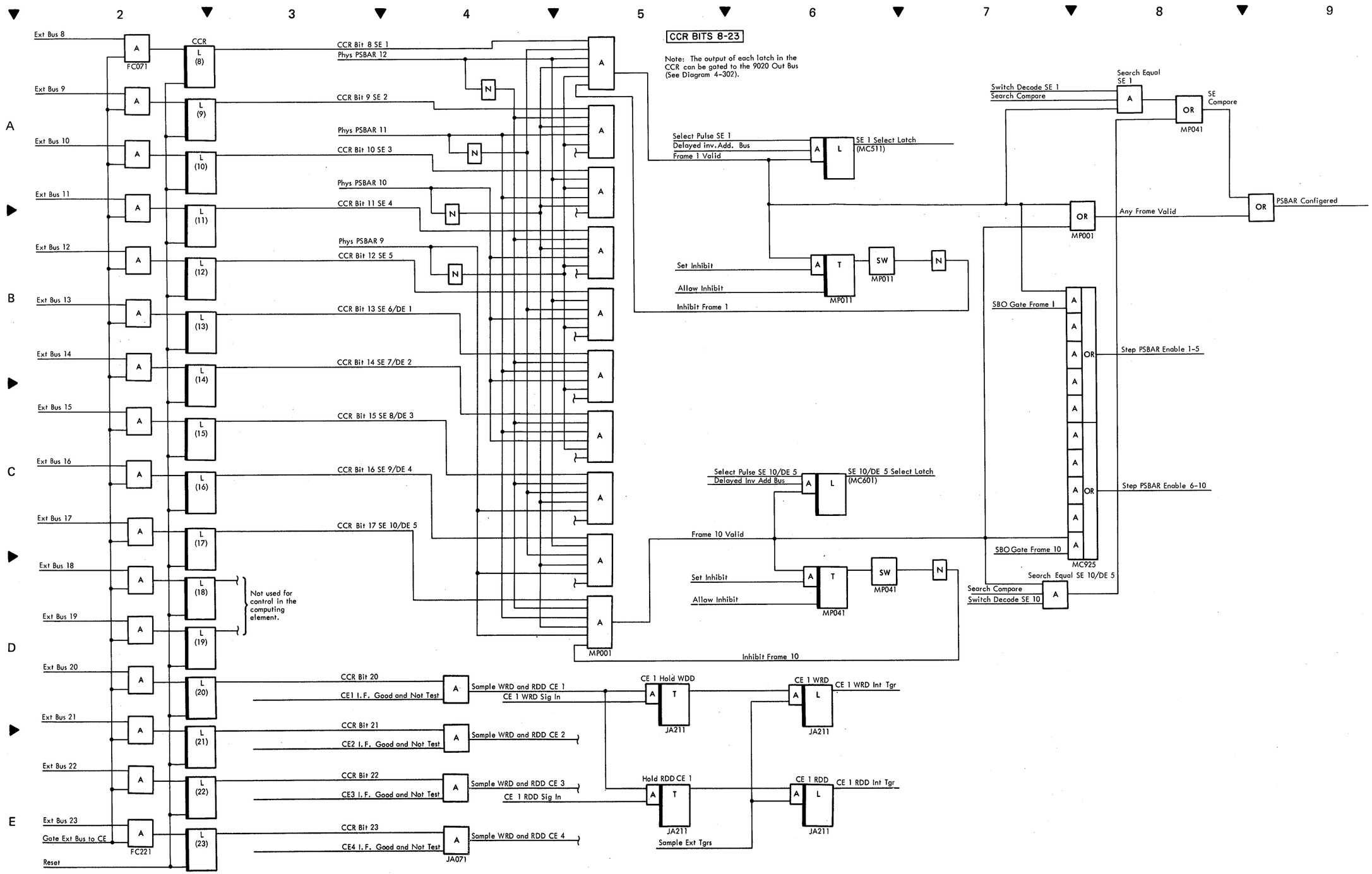


Diagram 4-210. CCR Output Logic and Control Paths (Sheet 2 of 3)

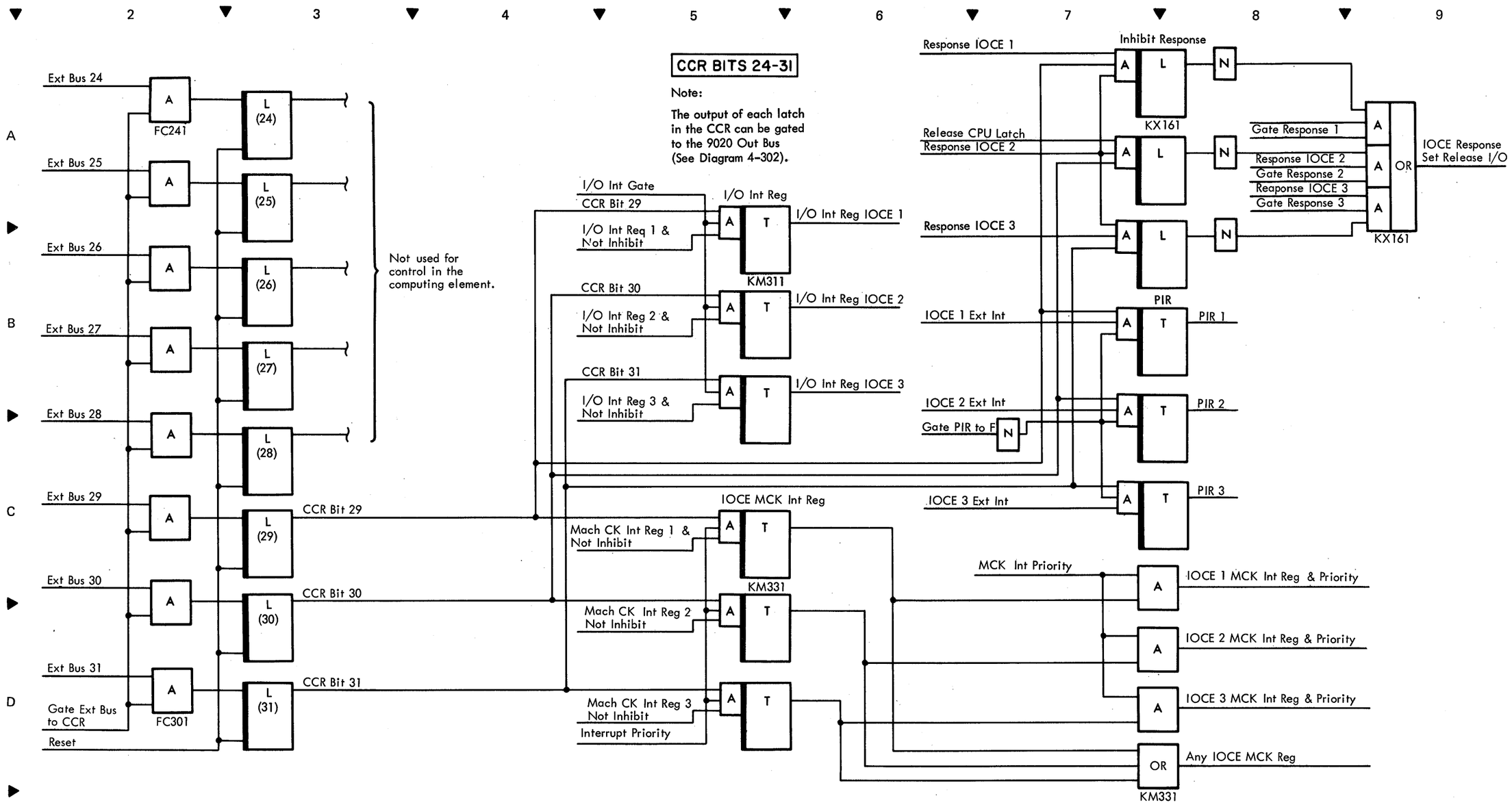
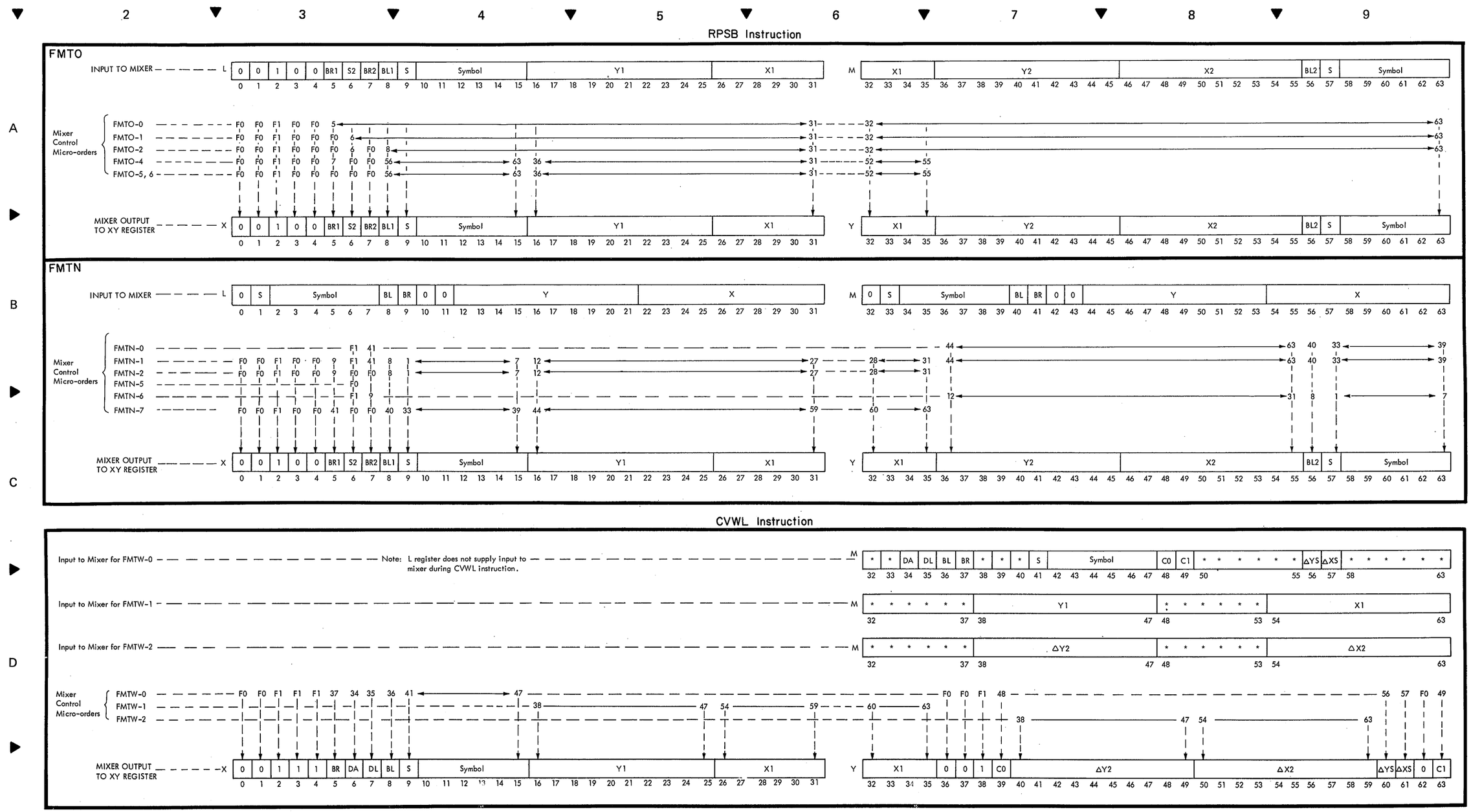


Diagram 4-210. CCR Output Logic and Control Paths (Sheet 3 of 3)



Notes:

1. To trace the origin of a mixer output bit: (1) select chart for specific instruction, RPSB or CVWL; (2) if RPSB is selected, refer to FMTO or FMTN portion of chart; (3) find bit to be traced in XY register and; (4) follow the line up to the micro-order being issued. For example, assume an RPSB instruction and an FMTN micro-order and assume bit 8 is to be traced. Refer to the RPSB instruction chart, FMTN portion, XY register. Find bit 8 in the XY register and follow the line up to the specific micro-order. If the specific micro-order is an FMTN-7, bit 8 originates from bit 40 of the LM-register. Note also that FMTN-0, 5, and 6 do not set bit 8 and that FMTN-1 and 2 set bit 8 from the input bit 8 in the LM register.
2. Parity for all XY bytes is predicted from LM data parity and LM parity bits.
3. XY register is reset on receipt of either FMTO; FMTN-1, -2, -7; or FMTW-0.

Legend:

1. F0 = Bit forced to 0
2. F1 = Bit forced to 1
3. BR = Brightness bit
   BL = Blink bit
   S = Symbol size
   DA = Dash
   DL = Dash length
   ΔYS = Sign of ΔY2
   ΔXS = Sign of ΔX2
   C0 = Character at major position
   C1 = Character at secondary position
   * = Not used

Diagram 4-211. LM to XY Reformatting via Mixer (Sheet 1 of 2)

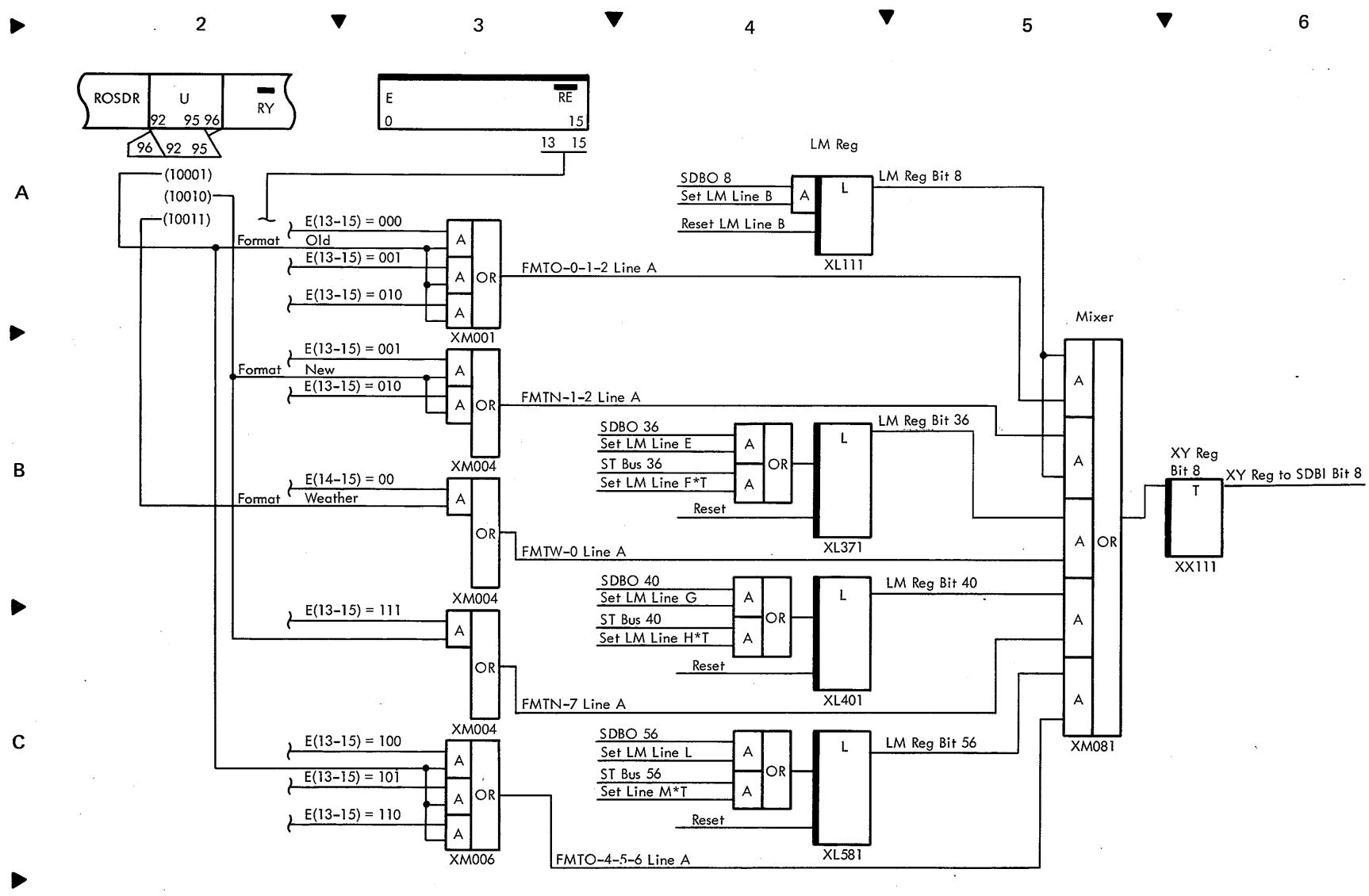


Diagram 4-211. LM to XY Reformatting via Mixer (Sheet 2 of 2)

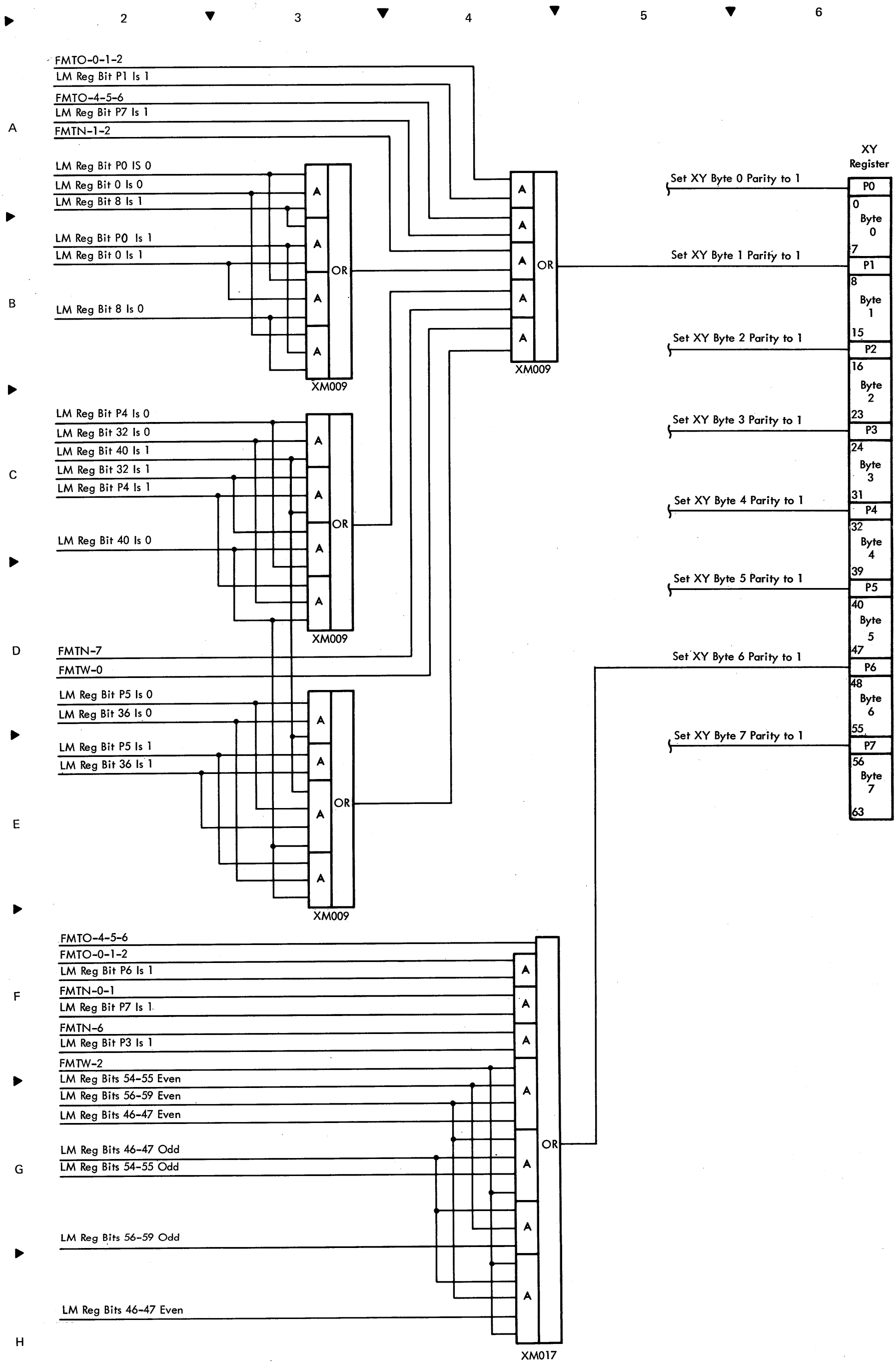


Diagram 4-212. XY Register Parity Prediction Logic

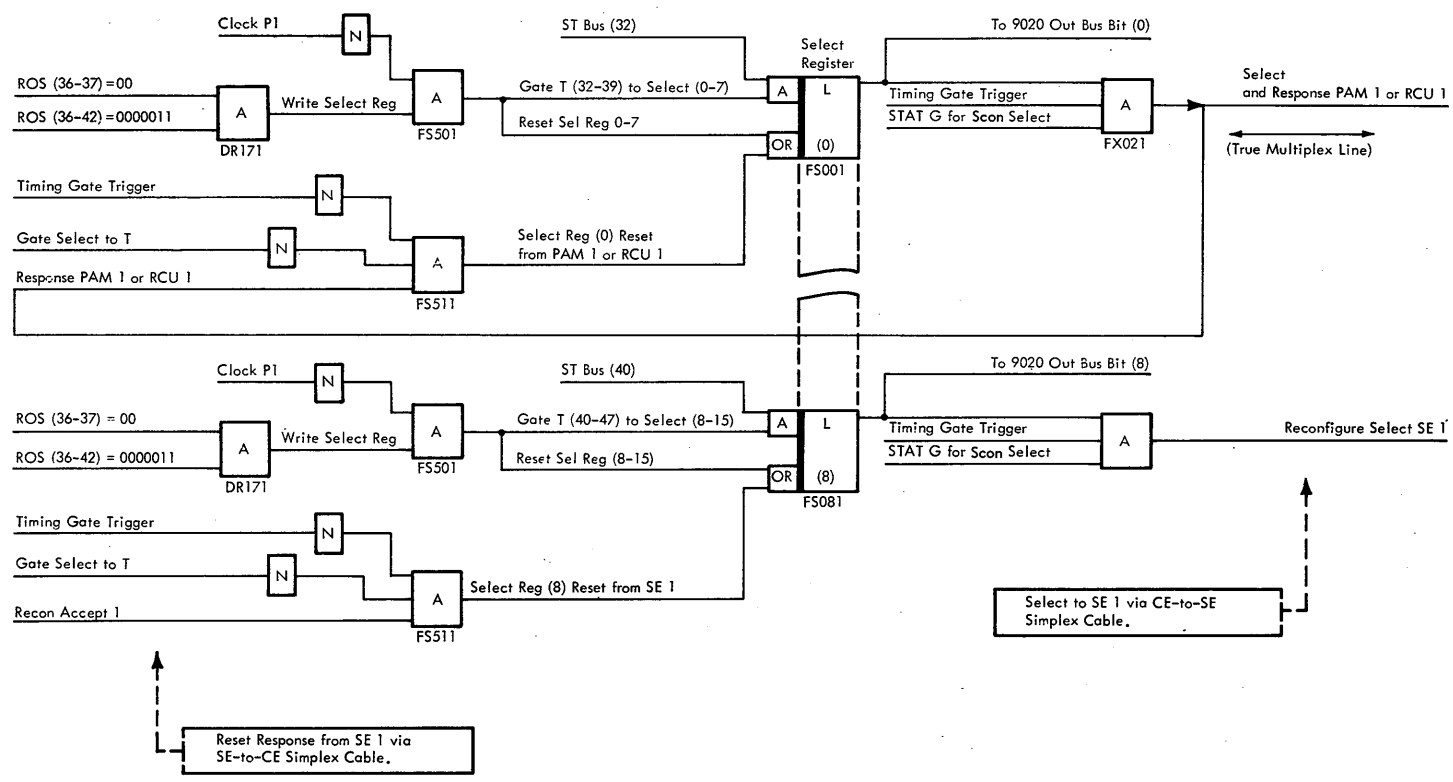


Diagram 4-213. Select Register - Select Signal Generation and Response Reset

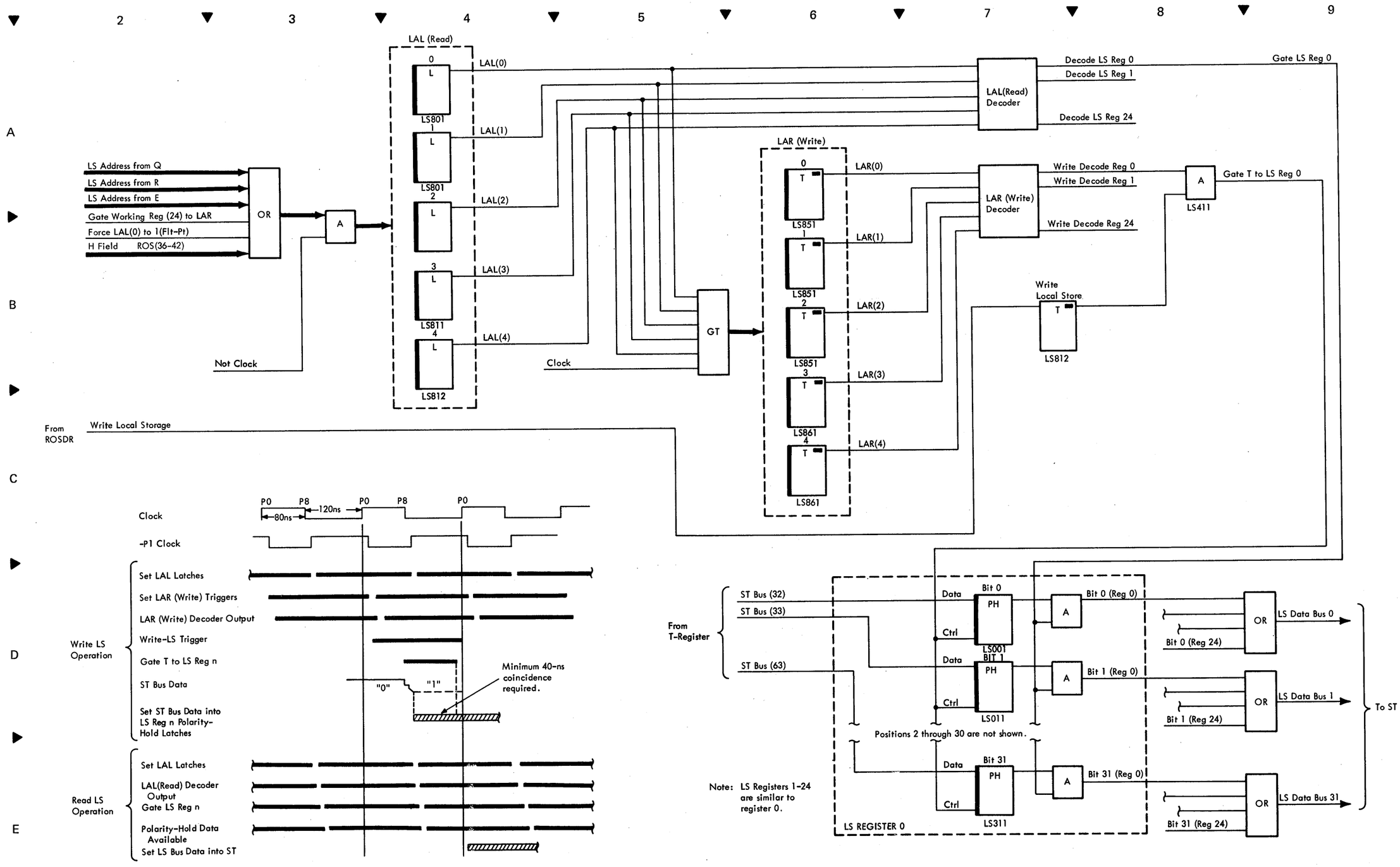


Diagram 4-301. Local Storage Read/Write Controls

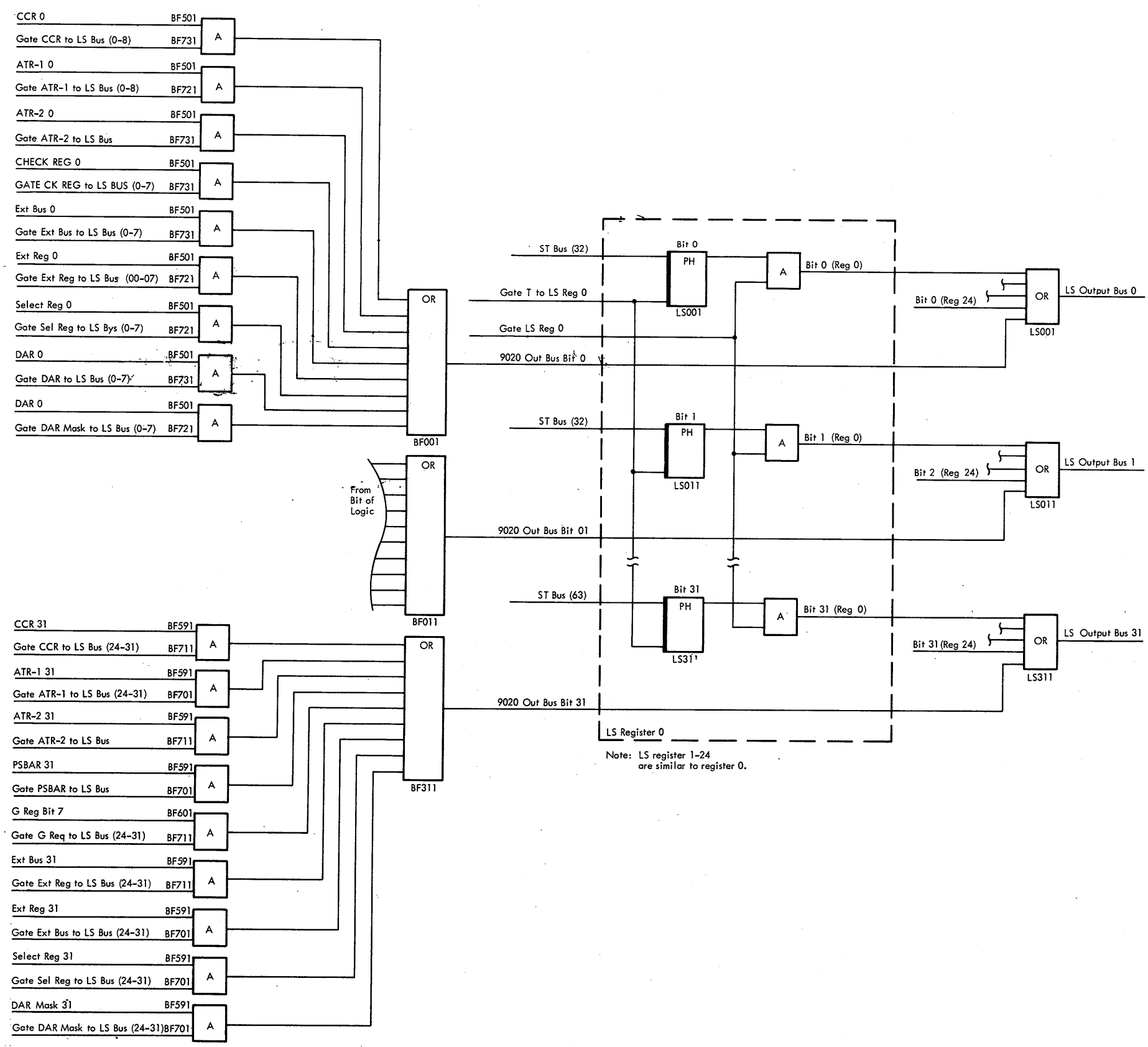


Diagram 4-302. 9020 Out Bus to LS Data Bus Gating Logic

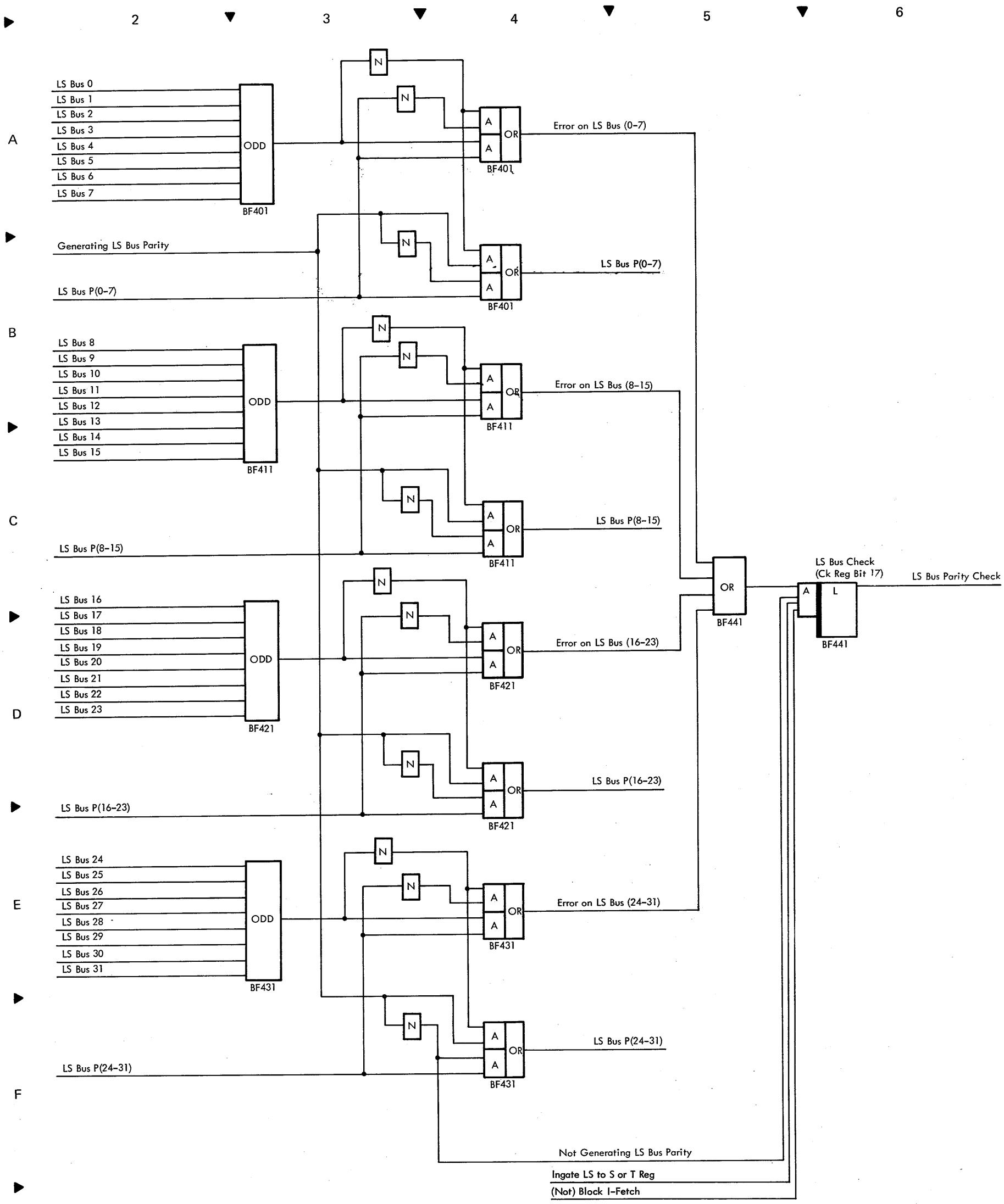


Diagram 4-303. LS Bus Parity Generation or Check

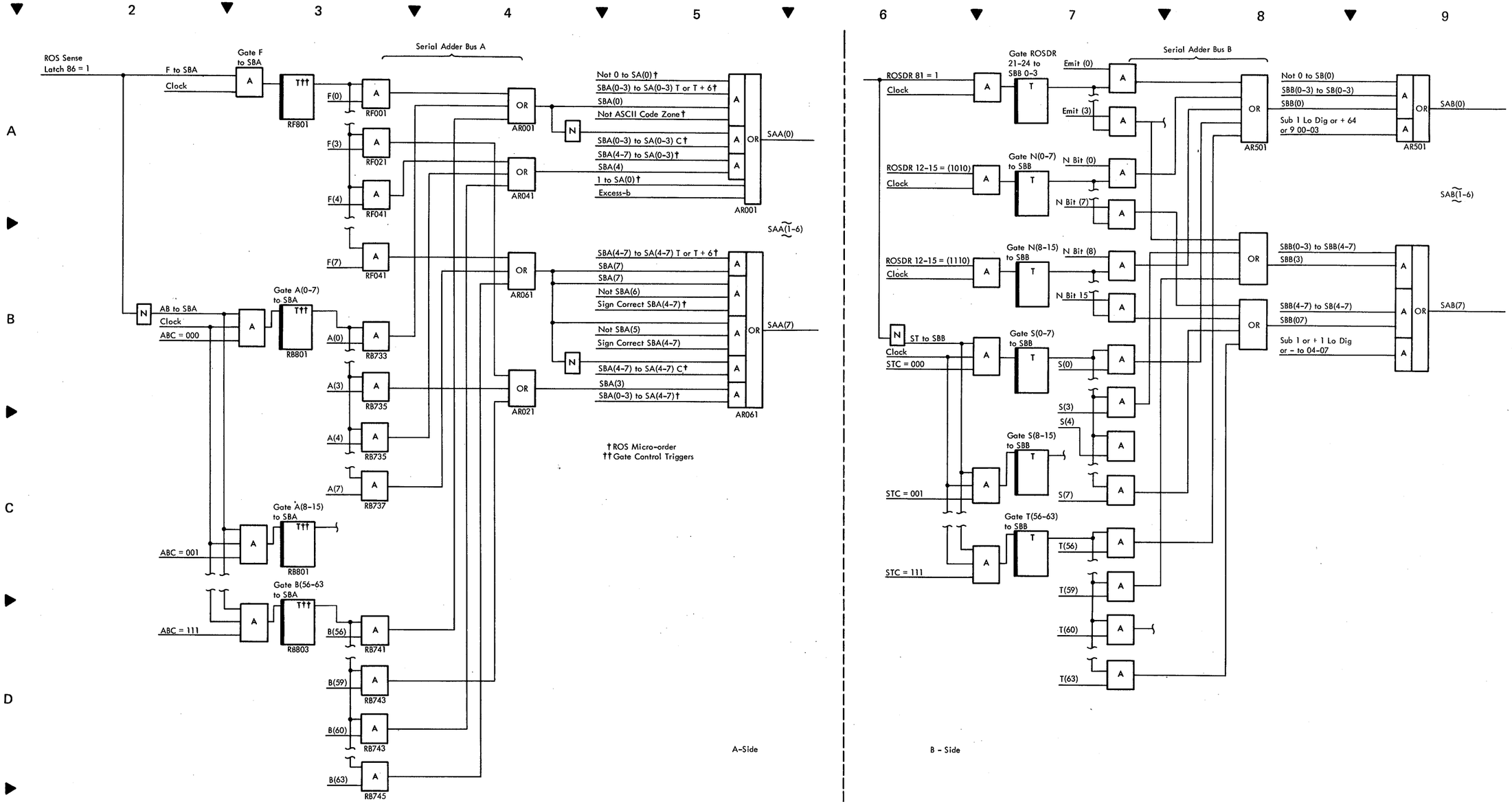


Diagram 4-401. Serial Adder Input Bus Logic

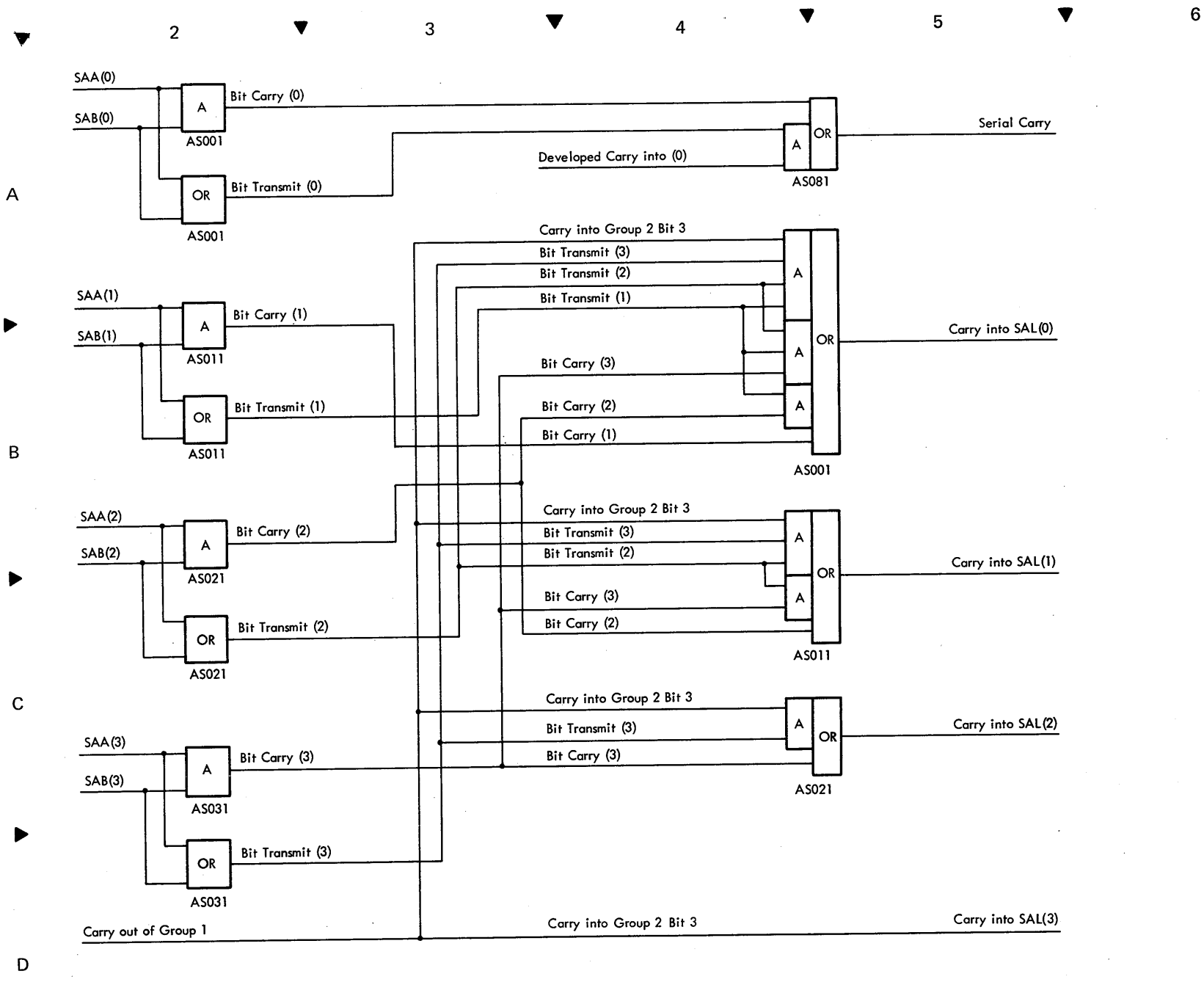


Diagram 4-402. Carry Lookahead Logic, SAL(0-3)

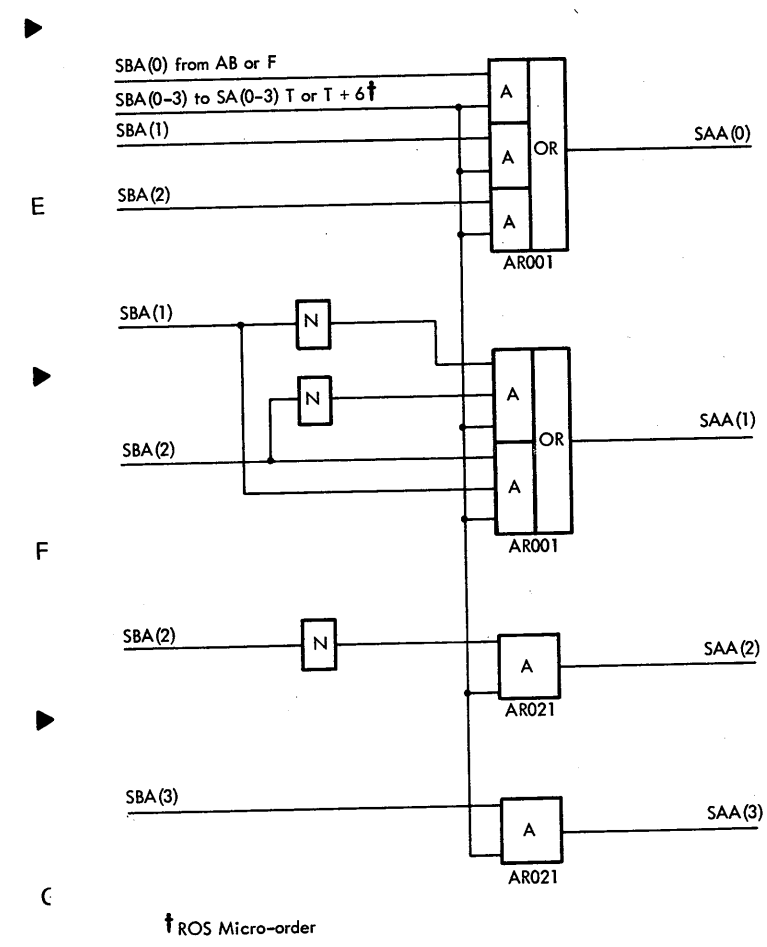


Diagram 4-403. Decimal Add 6 Logic

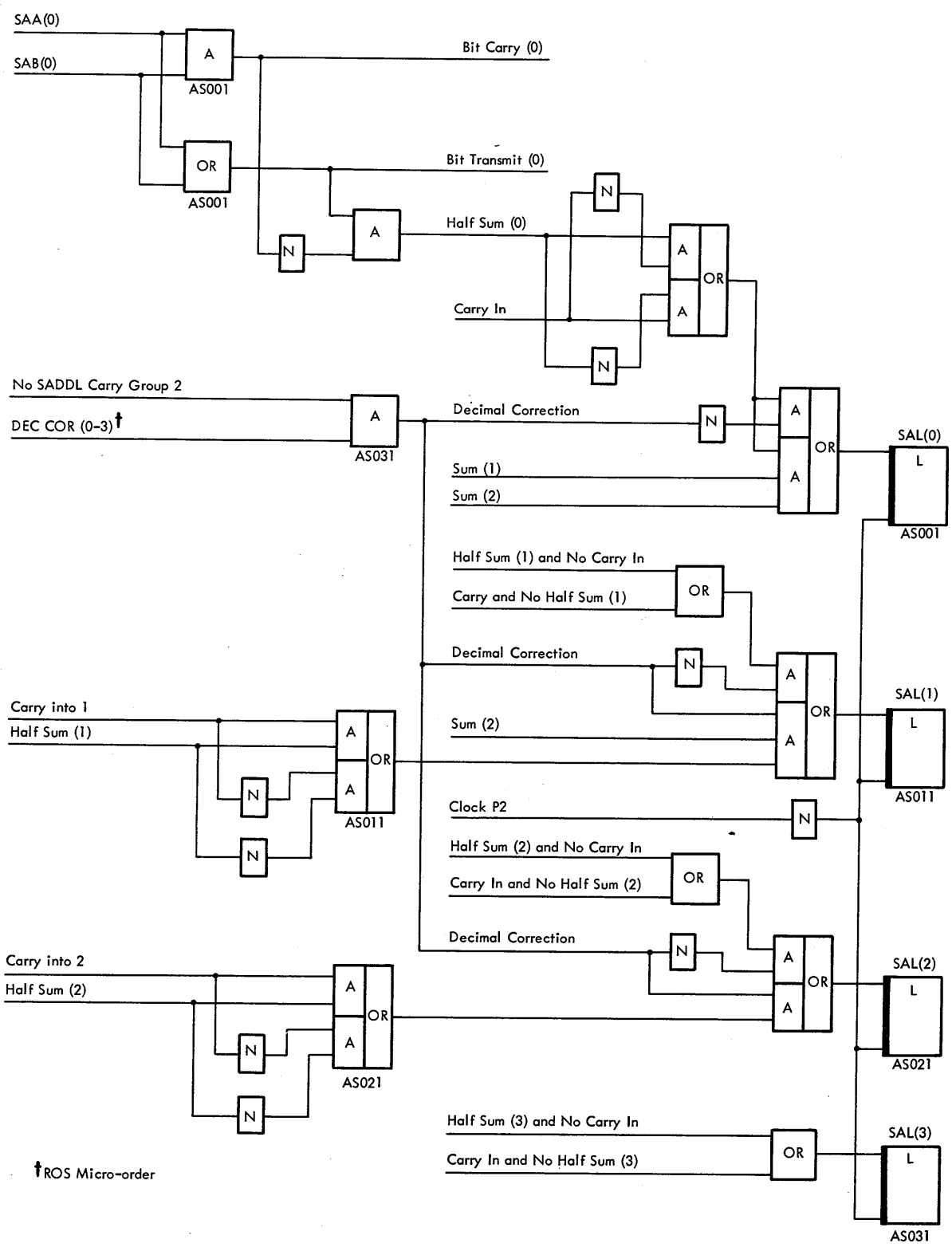


Diagram 4-404. Decimal Correction Logic For SAL (0-3)

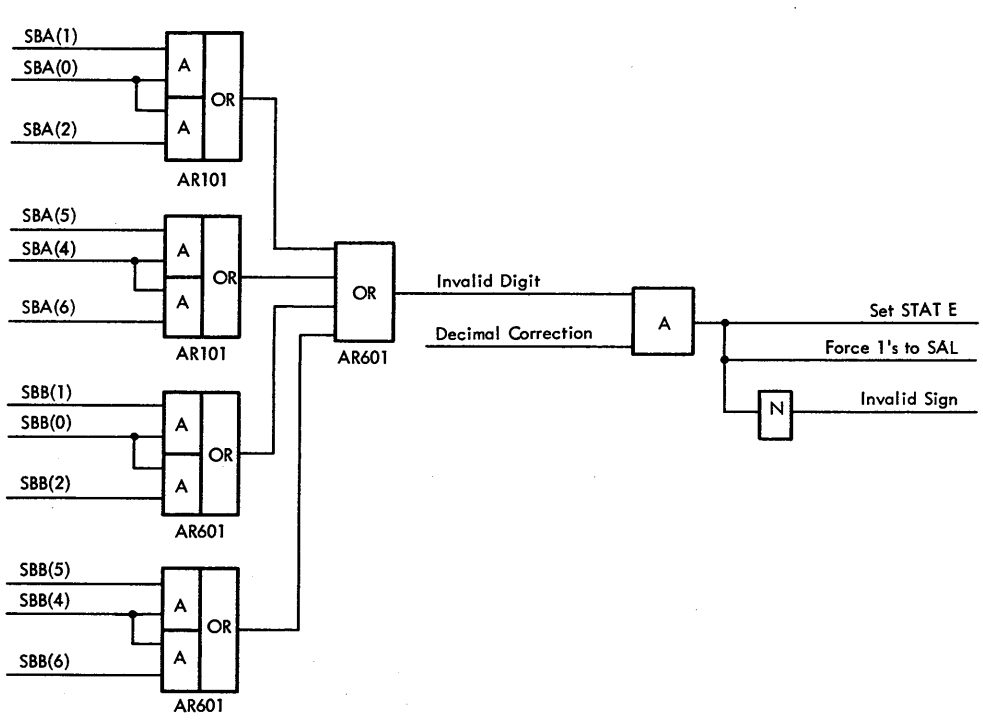


Diagram 4-405. Invalid Digit Logic

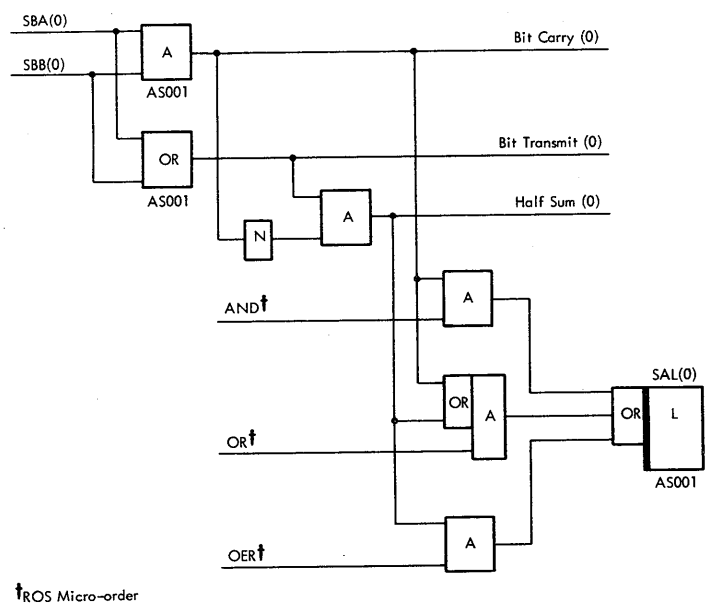


Diagram 4-406. Logical Functions, SAL (0)

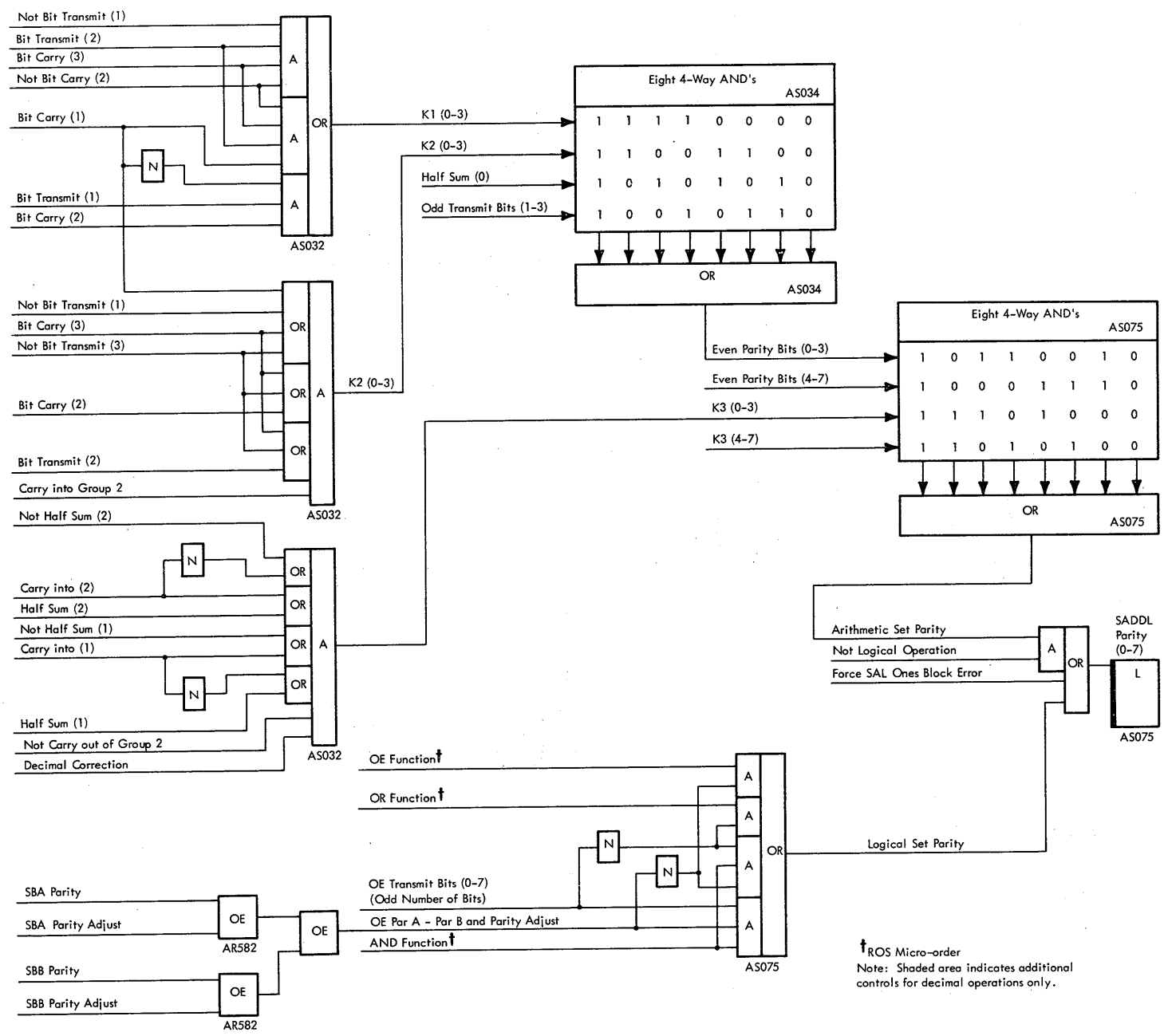


Diagram 4-407. Serial Adder Parity Predict Logic

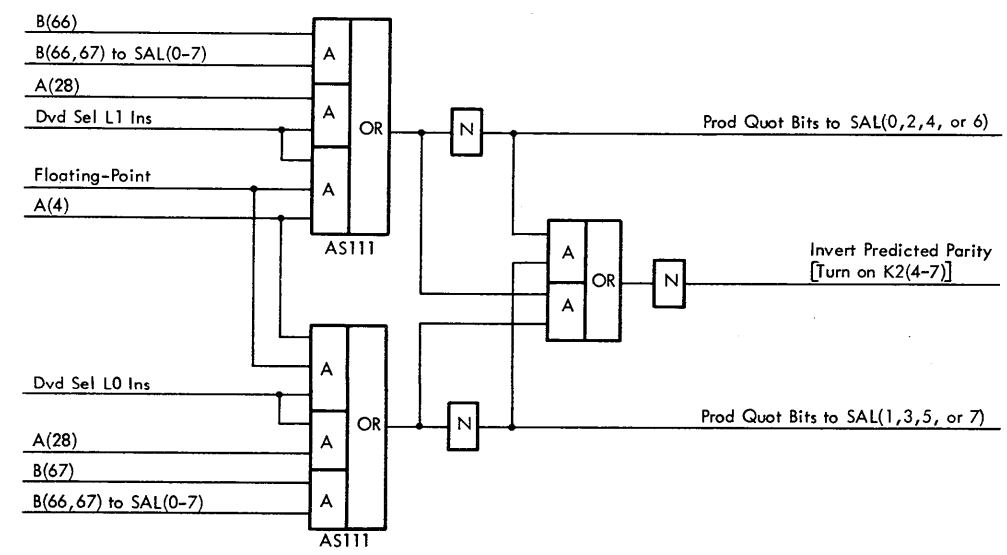
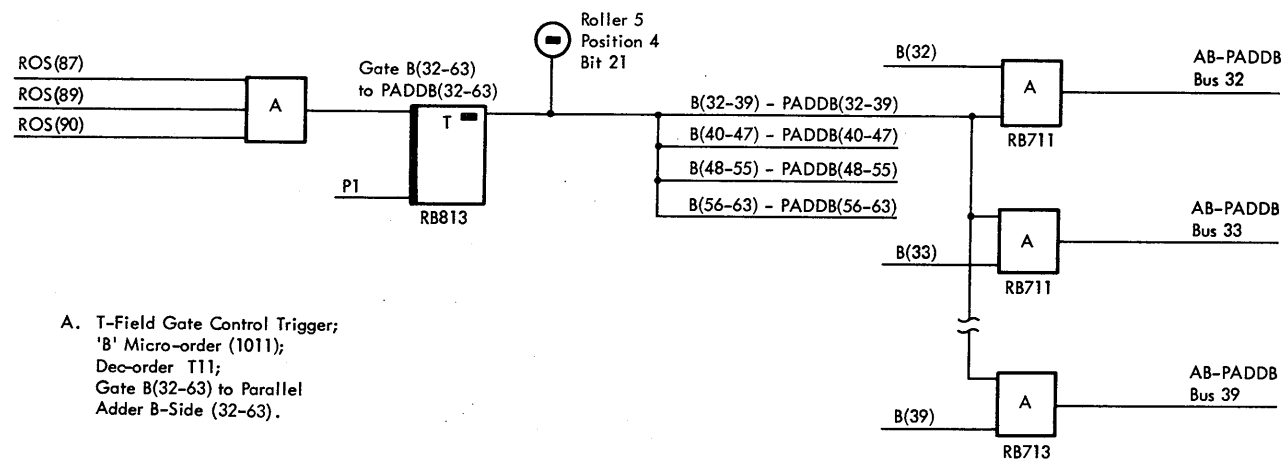


Diagram 4-408. Serial Adder Product-Quotient Bit Logic



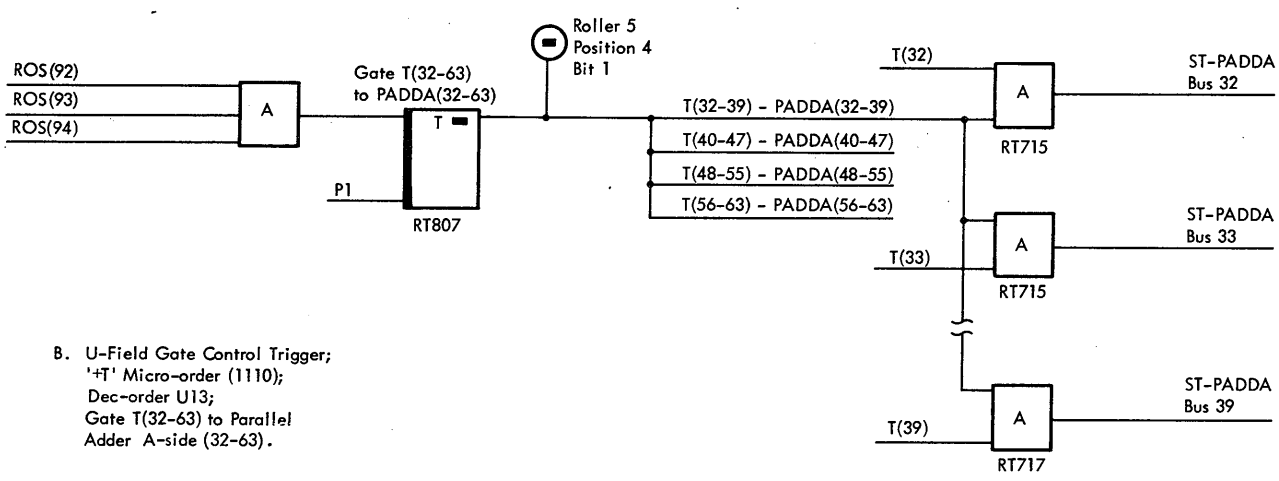
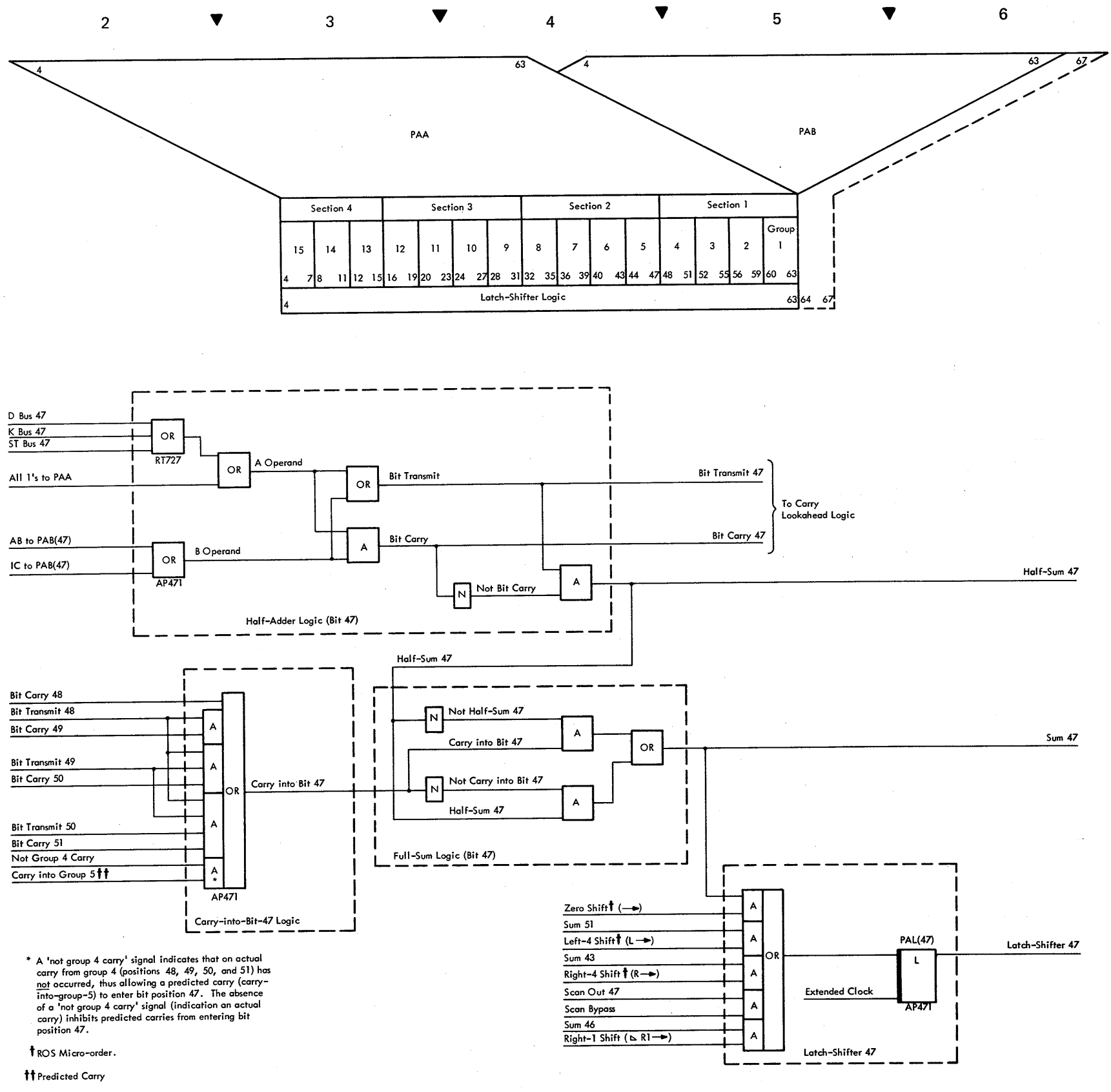


Diagram 4-409. Gate Control Triggers for 'B + T' Micro-order



* A 'not group 4 carry' signal indicates that on actual carry from group 4 (positions 48, 49, 50, and 51) has not occurred, thus allowing a predicted carry (carry-into-group-5) to enter bit position 47. The absence of a 'not group 4 carry' signal (indication an actual carry) inhibits predicted carries from entering bit position 47.

† ROS Micro-order.

†† Predicted Carry

Diagram 4-410. Parallel Adder Bit-Position Logic (Bit 47)

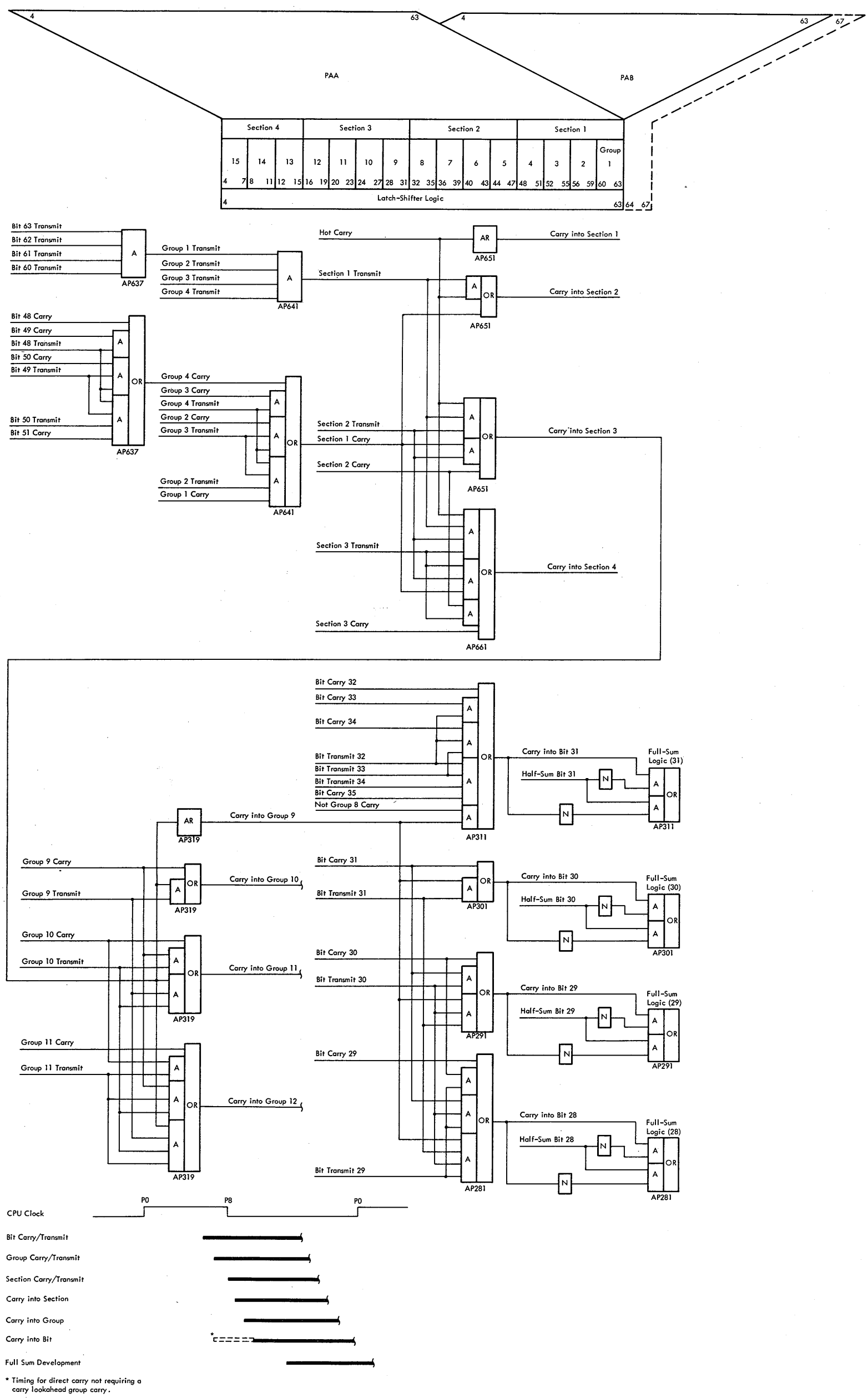


Diagram 4-411. Parallel Adder Carry Lookahead Logic

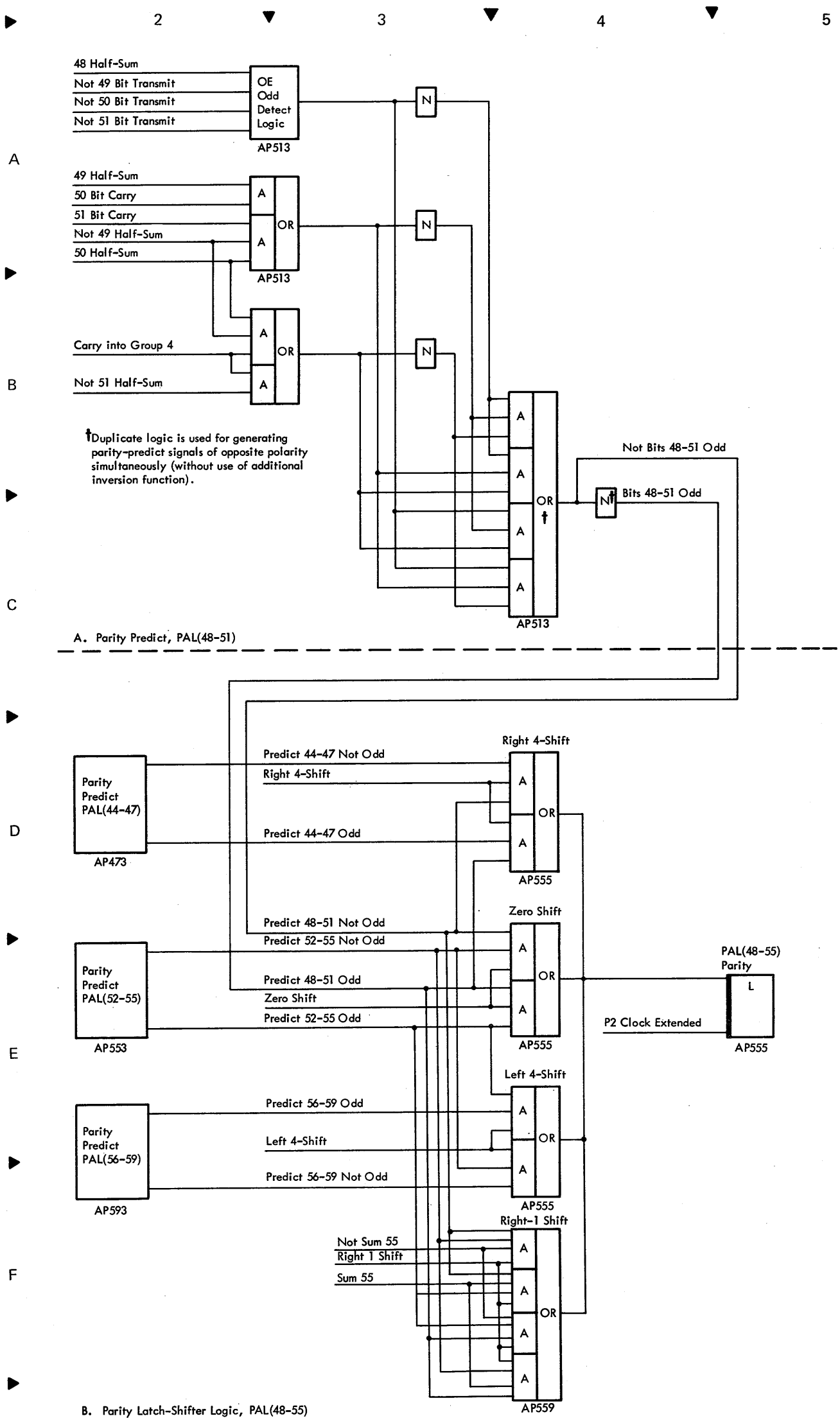


Diagram 4-412. Parity Generation, PAL (48-55)

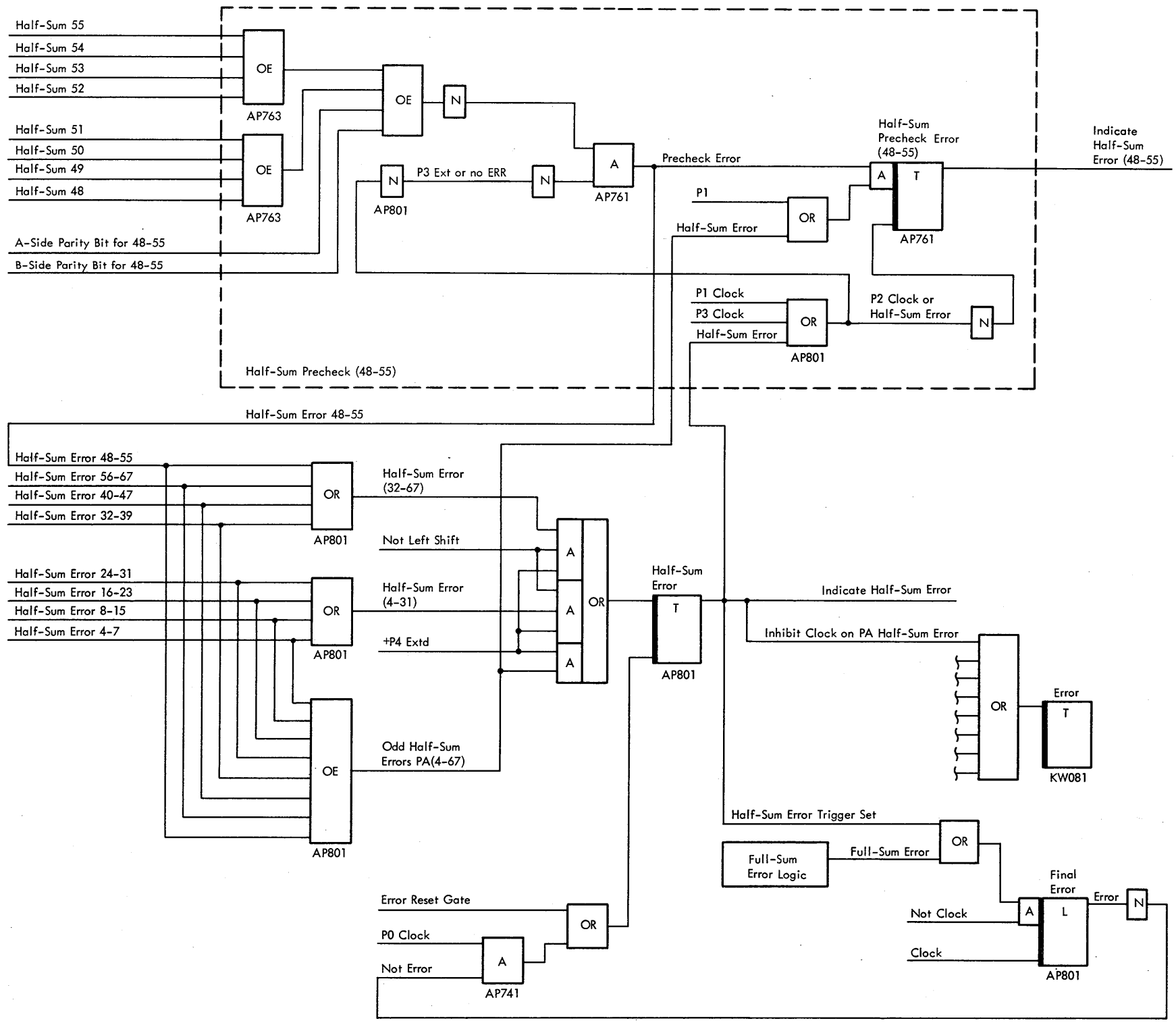


Diagram 4-413. Parallel Adder Half-Sum Checking Logic, PA (48-55)

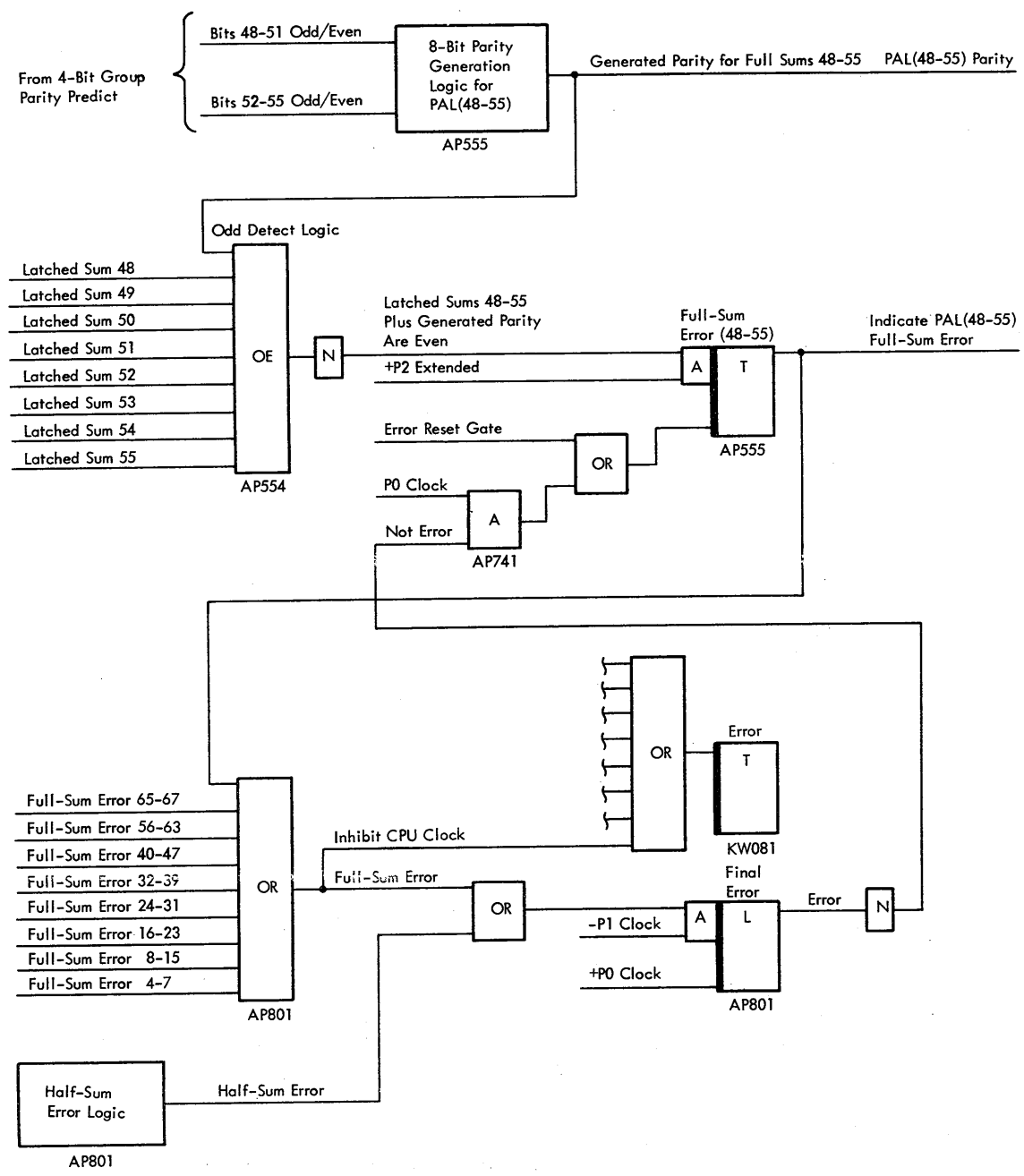


Diagram 4-414. Parallel Adder Full-Sum Checking Logic, PA(48-55)

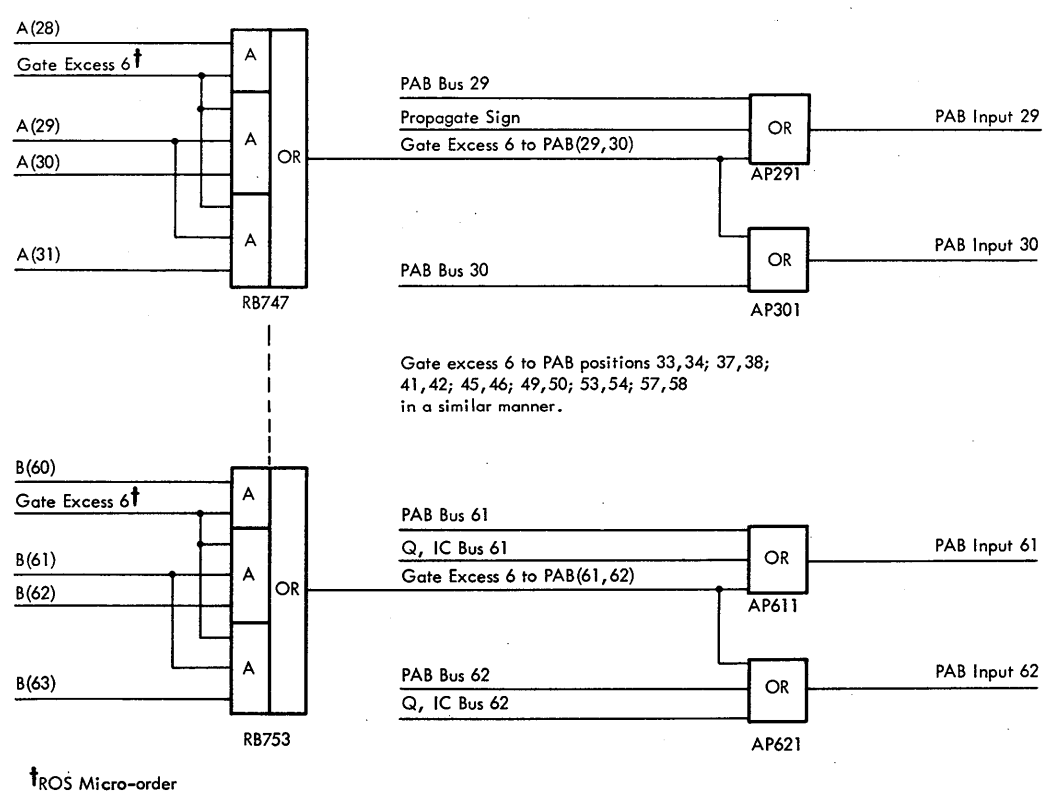


Diagram 4-415. Parallel Adder Excess 6 Logic

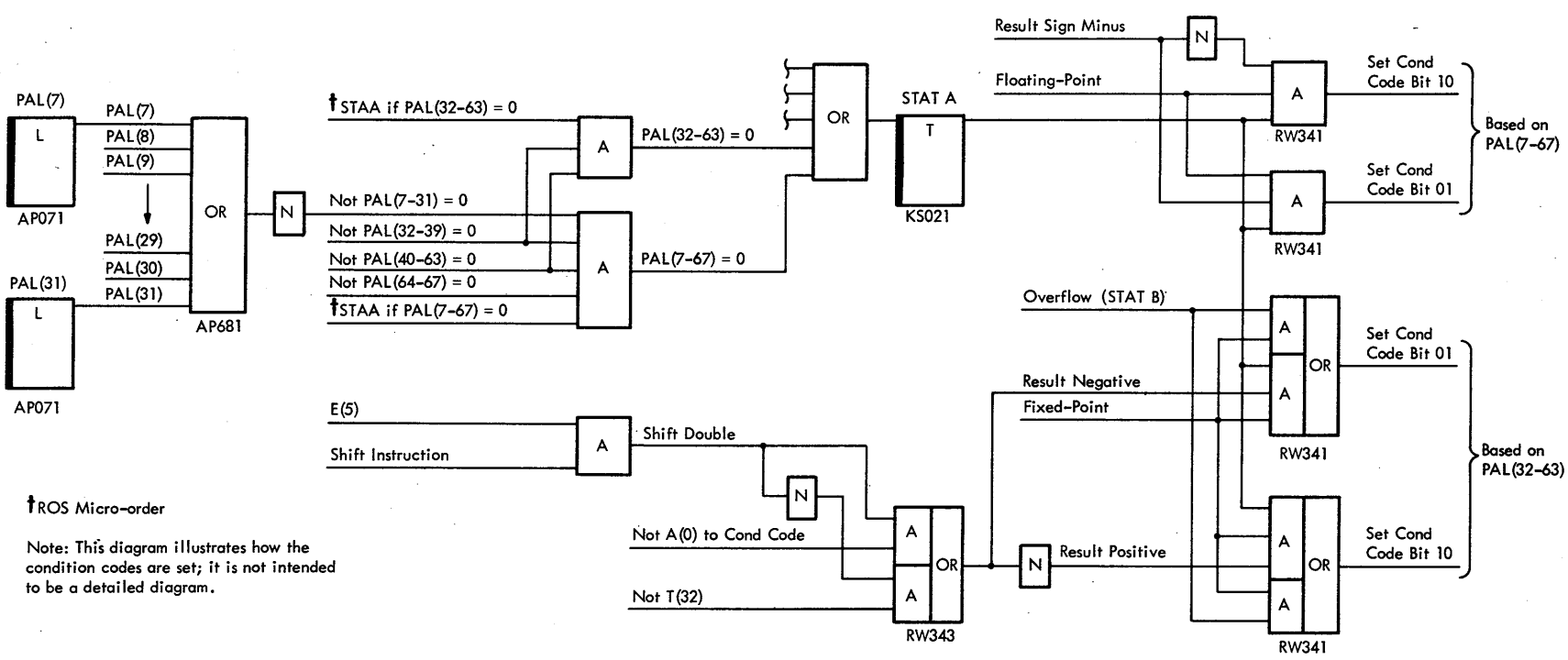


Diagram 4-416. Parallel Adder Set-Condition-Code Logic

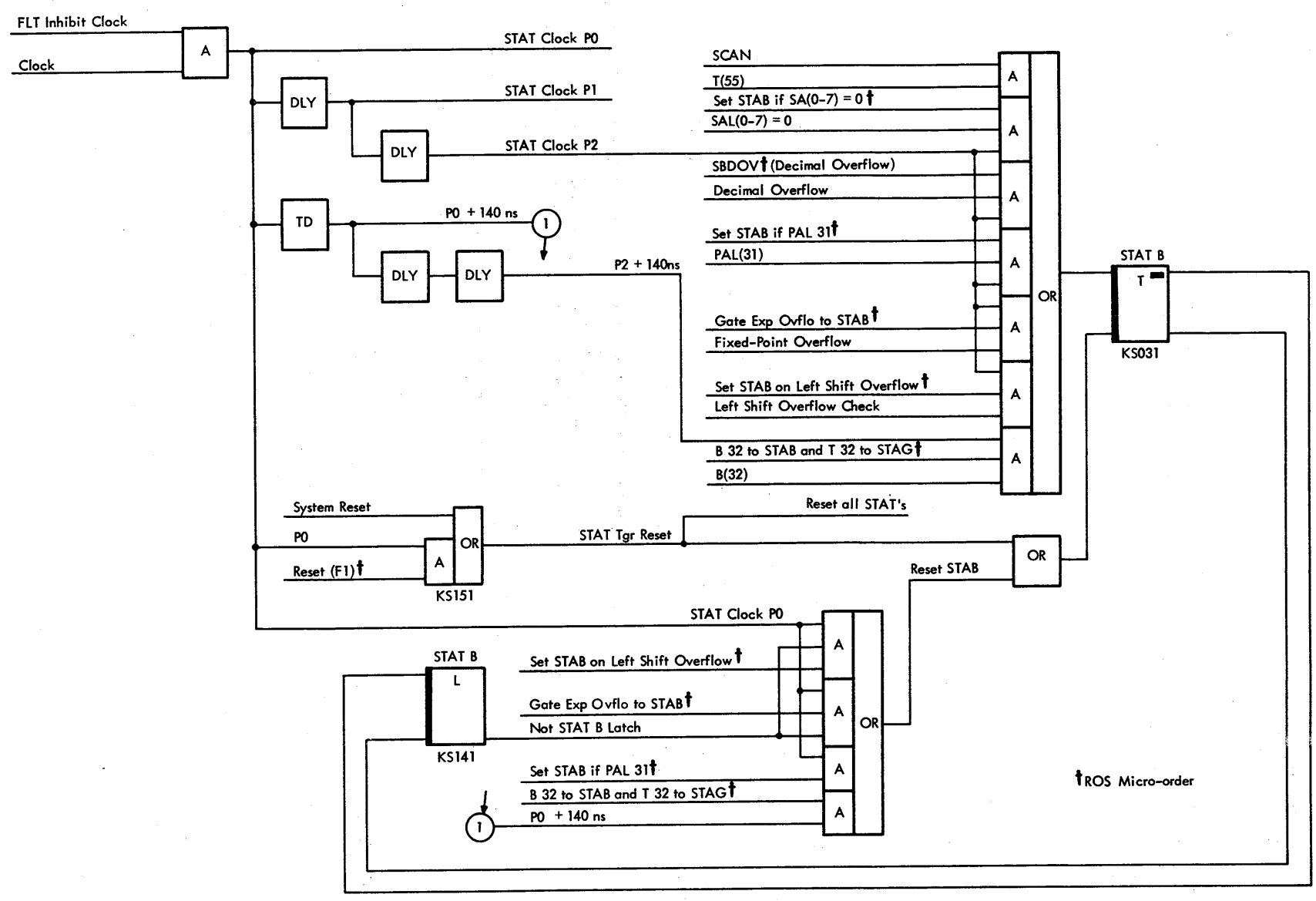


Diagram 4-501. STAT B Logic

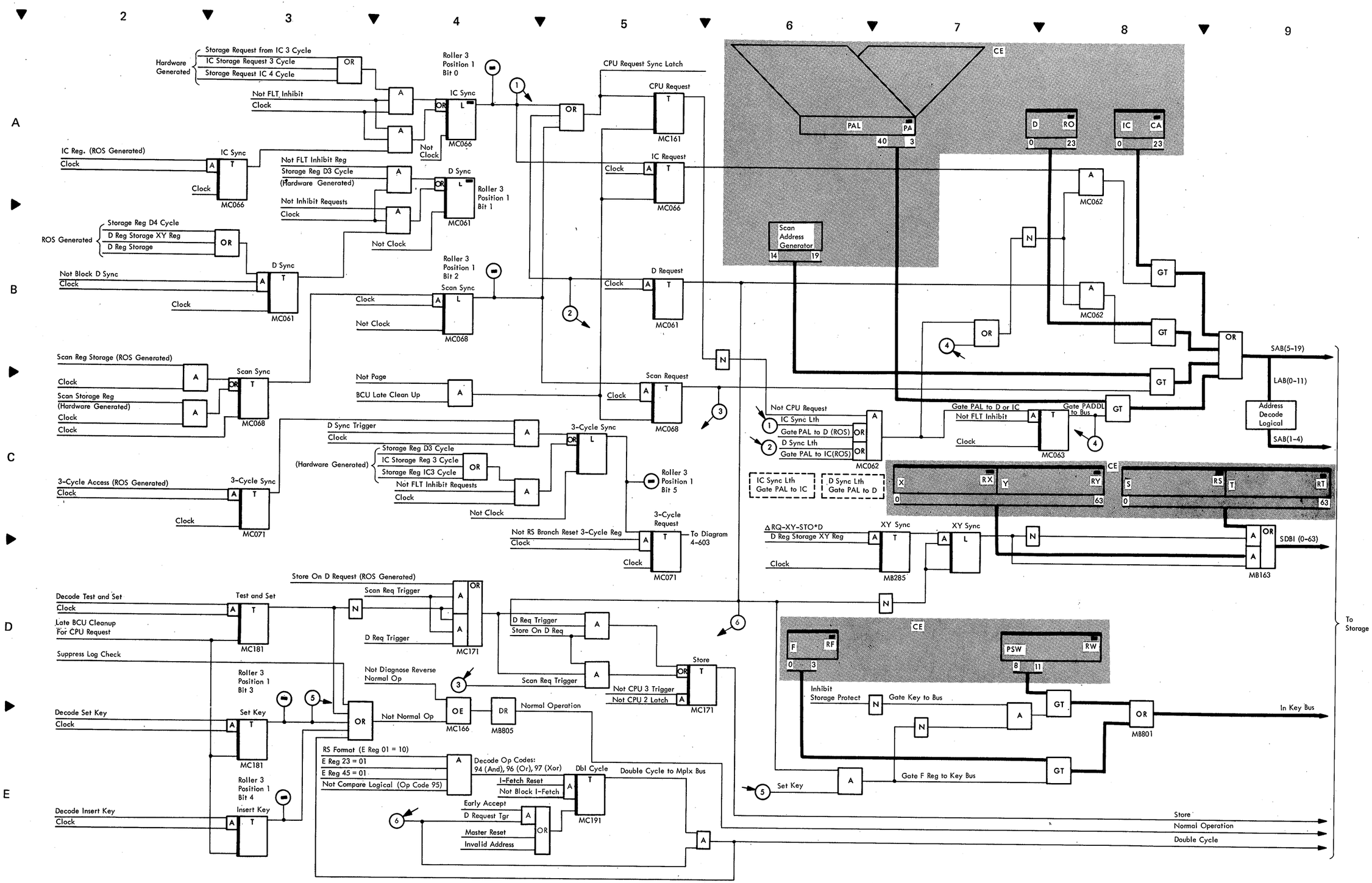


Diagram 4-601. SCI Request Sensing and Gating Logic

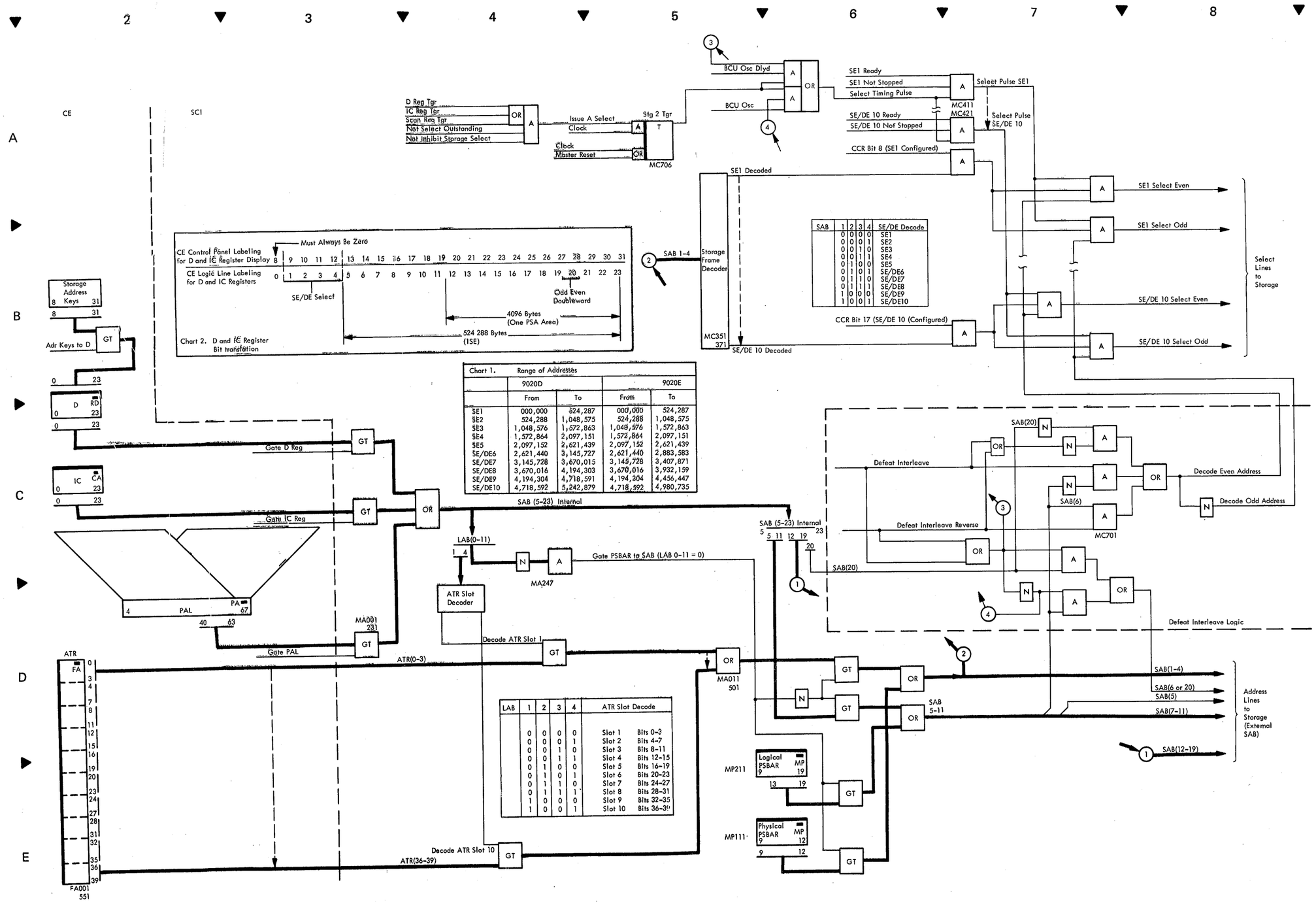


Chart 1. Range of Addresses	9020D		9020E	
	From	To	From	To
SE1	000,000	524,287	000,000	524,287
SE2	524,288	1,048,575	524,288	1,048,575
SE3	1,048,576	1,572,863	1,048,576	1,572,863
SE4	1,572,864	2,097,151	1,572,864	2,097,151
SE5	2,097,152	2,621,439	2,097,152	2,621,439
SE/DE6	2,621,440	3,145,727	2,621,440	2,883,583
SE/DE7	3,145,728	3,670,015	3,145,728	3,407,871
SE/DE8	3,670,016	4,194,303	3,670,016	3,932,159
SE/DE9	4,194,304	4,718,591	4,194,304	4,456,447
SE/DE10	4,718,592	5,242,879	4,718,592	4,980,735

SAB	1	2	3	4	SE/DE Decode
	0	0	0	0	SE1
	0	0	0	1	SE2
	0	0	1	0	SE3
	0	0	1	1	SE4
	0	1	0	0	SE5
	0	1	0	1	SE/DE6
	0	1	1	0	SE/DE7
	0	1	1	1	SE/DE8
	1	0	0	0	SE/DE9
	1	0	0	1	SE/DE10

LAB	1	2	3	4	ATR Slot Decode	
	0	0	0	0	Slot 1	Bits 0-3
	0	0	0	1	Slot 2	Bits 4-7
	0	0	1	0	Slot 3	Bits 8-11
	0	0	1	1	Slot 4	Bits 12-15
	0	1	0	0	Slot 5	Bits 16-19
	0	1	0	1	Slot 6	Bits 20-23
	0	1	1	0	Slot 7	Bits 24-27
	0	1	1	1	Slot 8	Bits 28-31
	1	0	0	0	Slot 9	Bits 32-35
	1	0	0	1	Slot 10	Bits 36-39

Diagram 4-602. Address Decode and Gating Logic

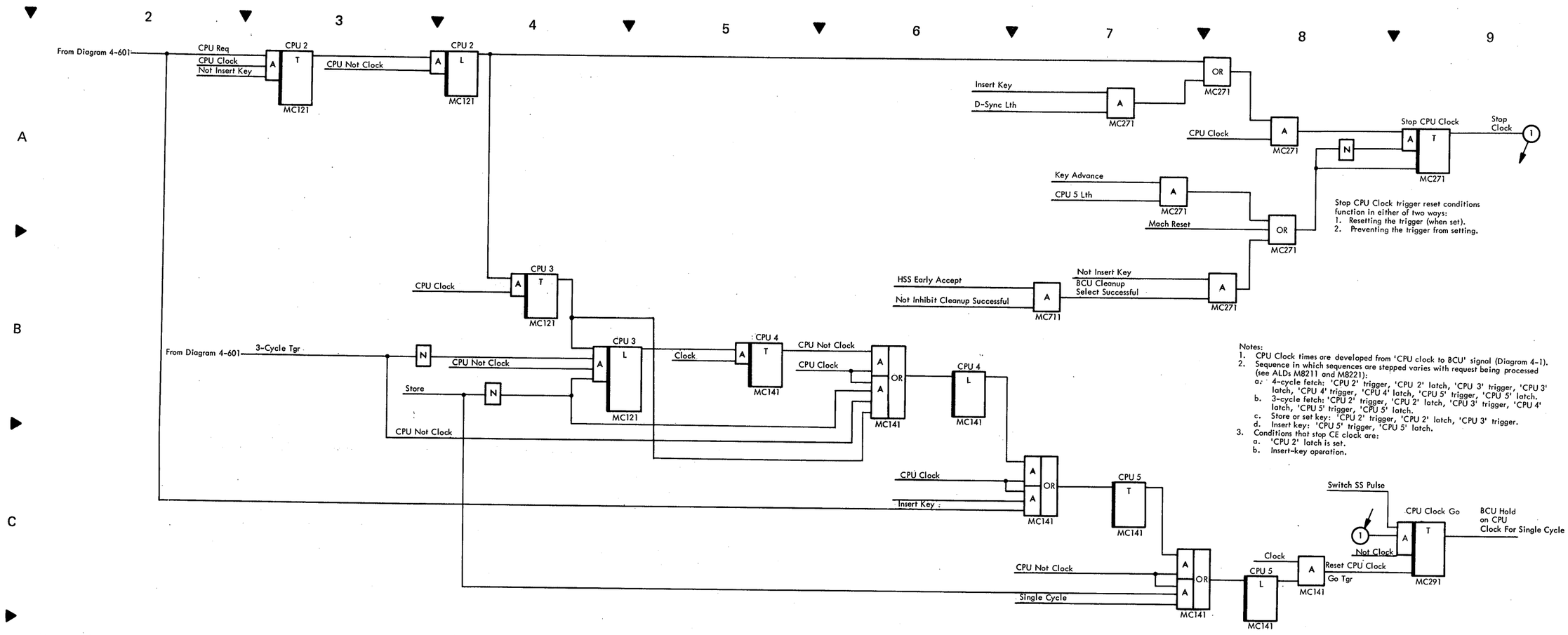


Diagram 4-603. SCI Control Logic for CE Clock

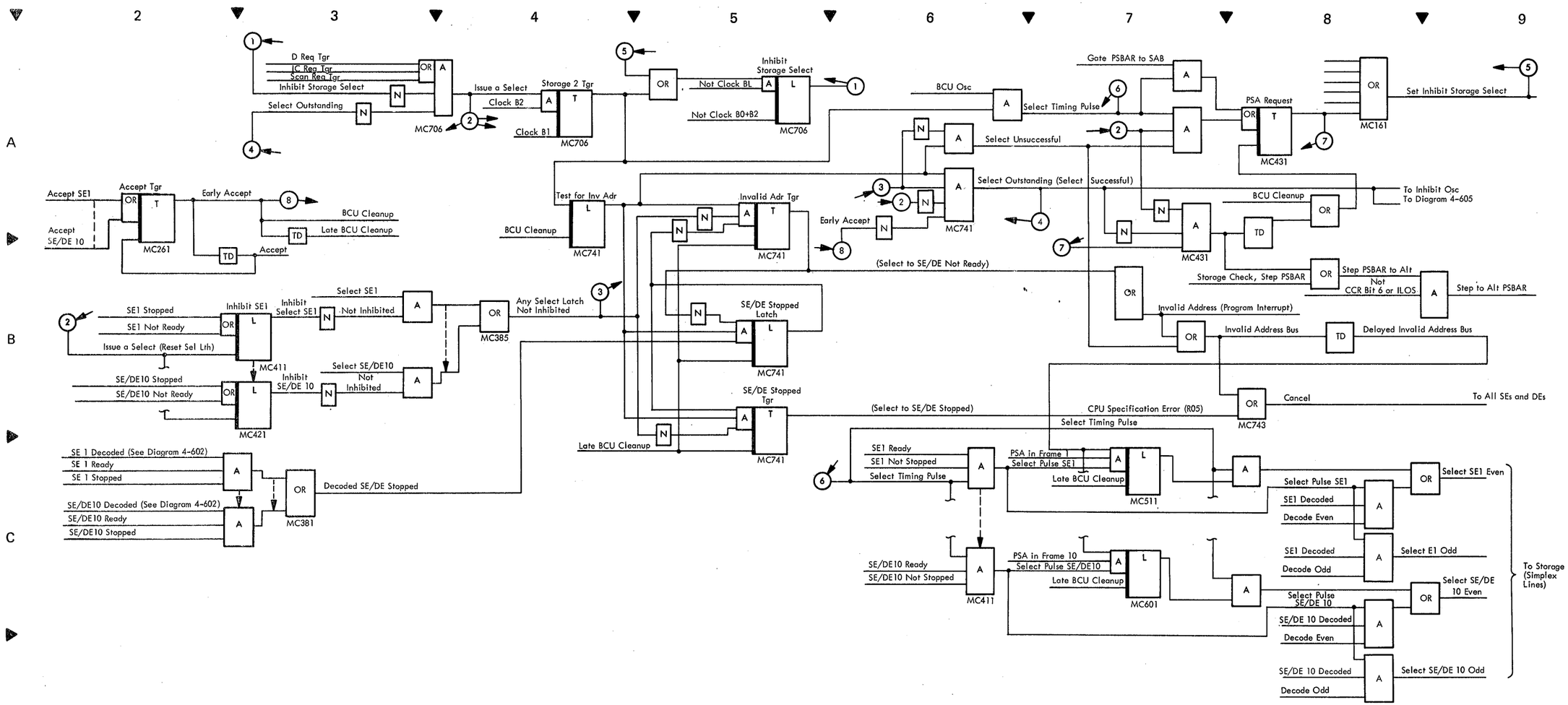


Diagram 4-604. Invalid Address and Frame Stopped Logic (Sheet 1 of 2)

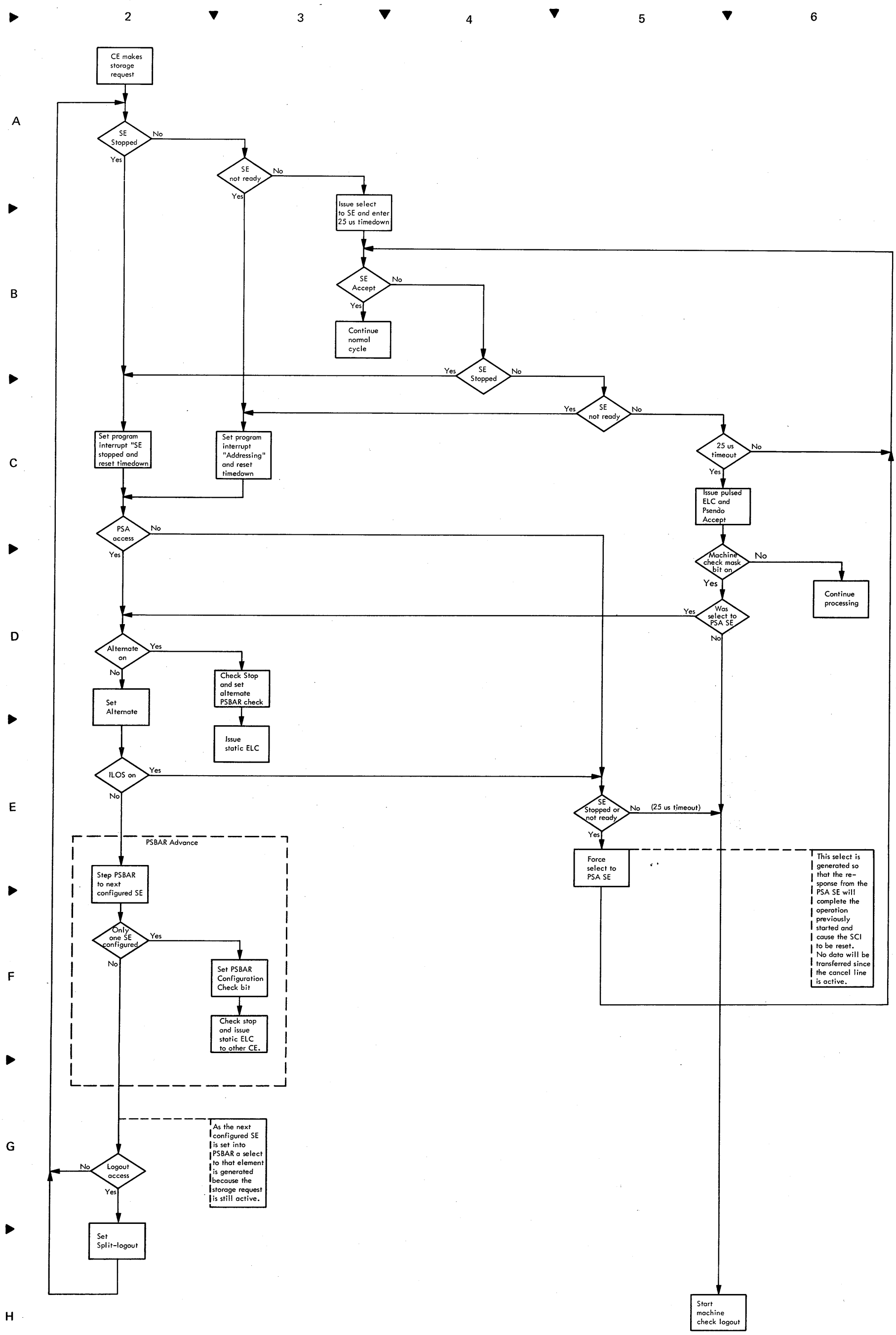
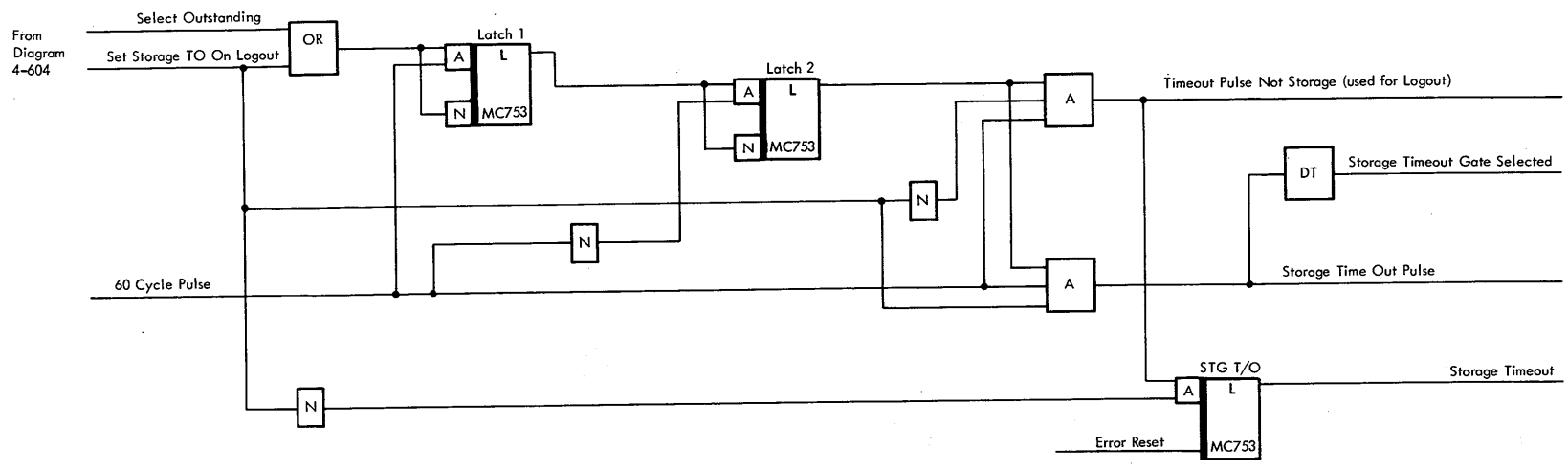
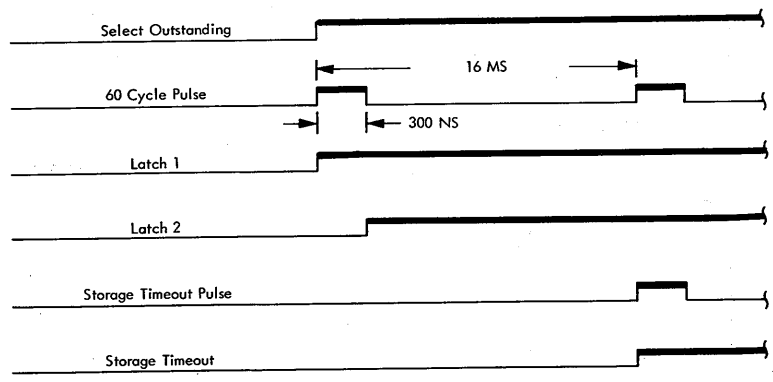


Diagram 4-604. Invalid Address and Frame Stopped Logic (Sheet 2 of 2)





Notes:
1. 'Storage timeout' is activated if 'select outstanding' remains active through two '60-cycle pulses'.
2. 'Select outstanding' may come at any time; the example shown is for the least amount of time necessary to set 'storage timeout'.
3. 'Select outstanding' is deactivated by 'accept' from storage.

Diagram 4-605. Storage Timeout Logic

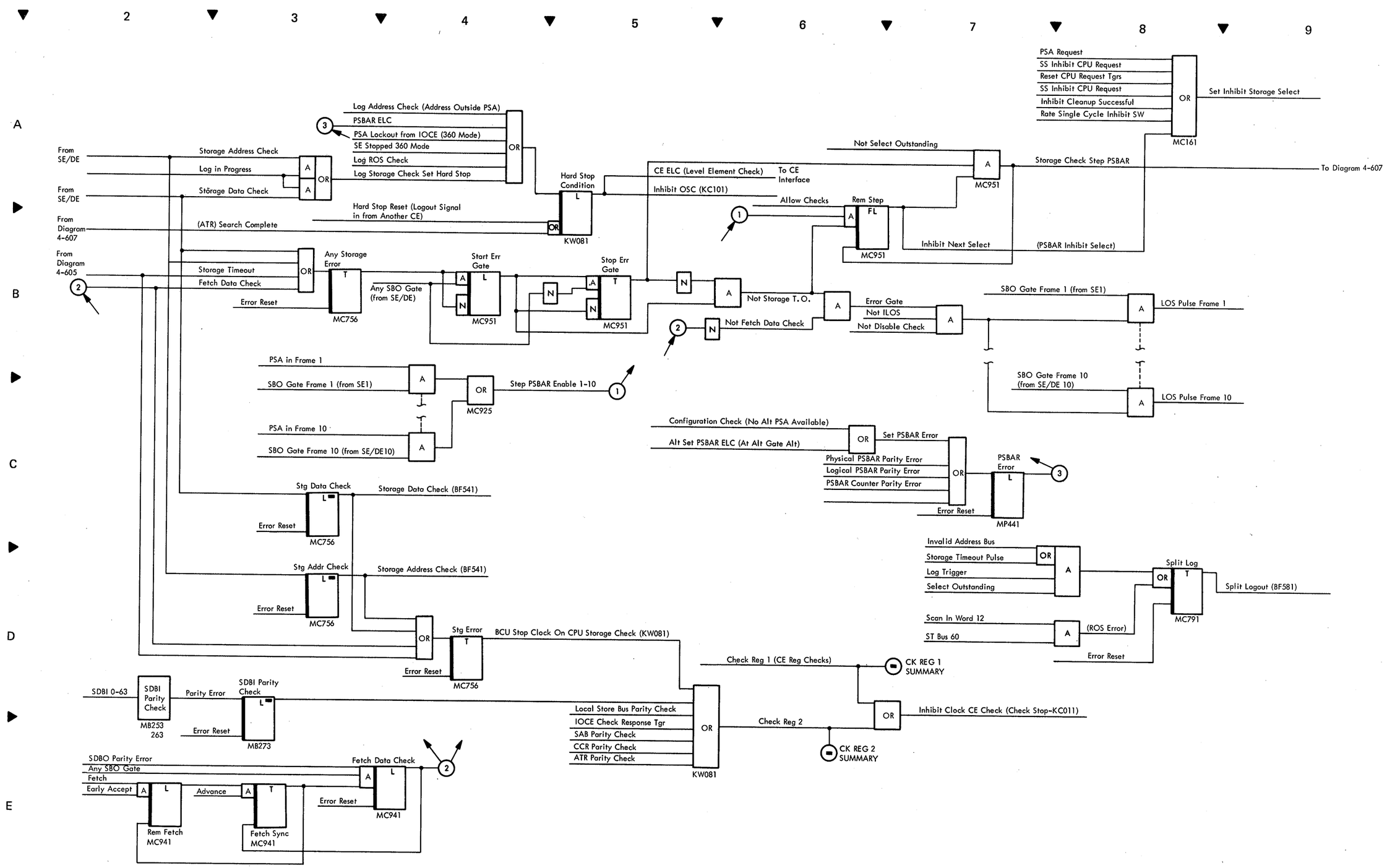
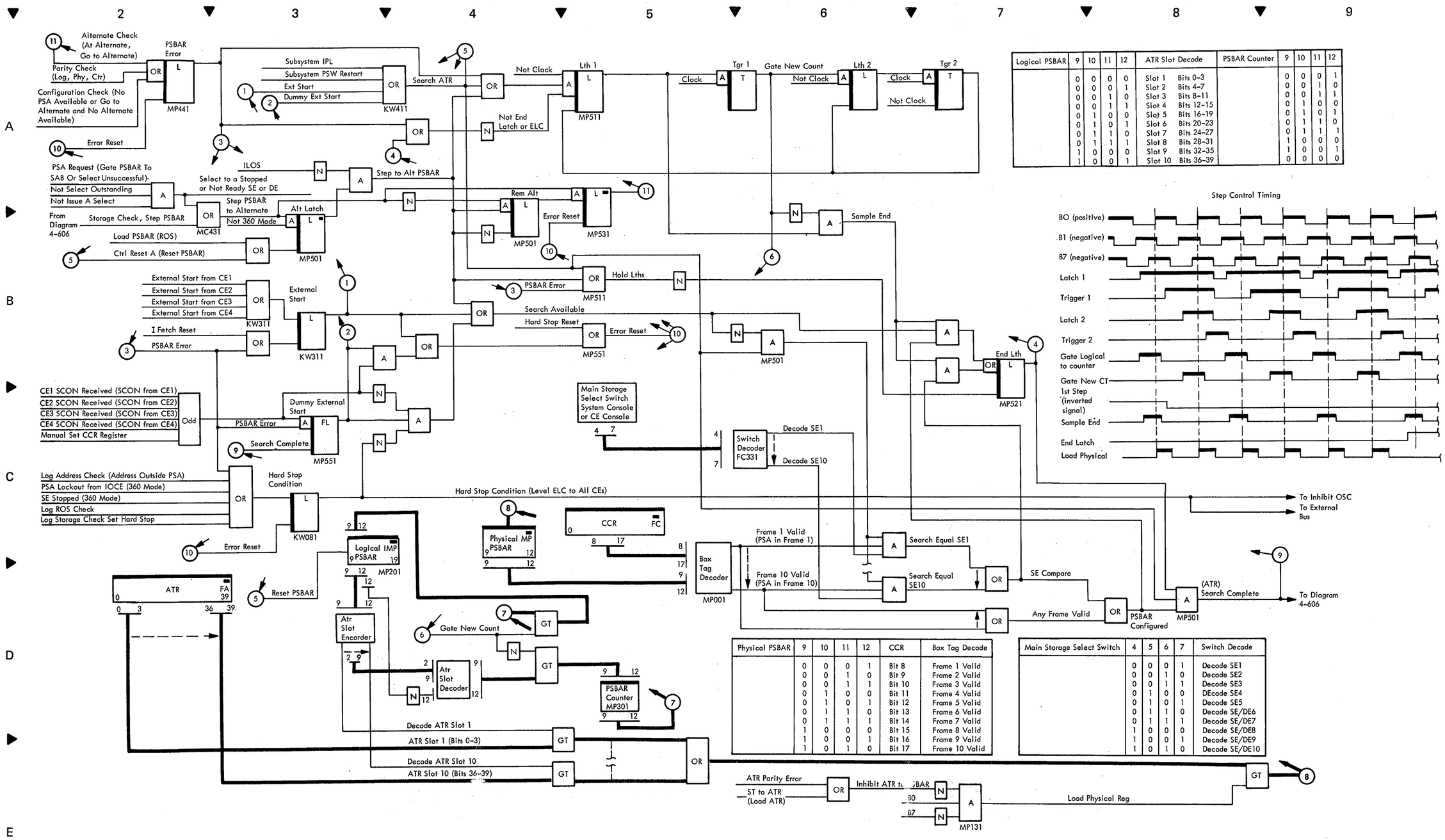


Diagram 4-606. Error Handling Logic



Logical PSBAR	9	10	11	12	ATR Slot Decode		PSBAR Counter	9	10	11	12
	0	0	0	0	Slot 1	Bits 0-3		0	0	0	1
	0	0	0	1	Slot 2	Bits 4-7		0	0	1	0
	0	0	1	0	Slot 3	Bits 8-11		0	0	1	1
	0	0	1	1	Slot 4	Bits 12-15		0	1	0	0
	0	1	0	0	Slot 5	Bits 16-19		0	1	0	1
	0	1	0	1	Slot 6	Bits 20-23		0	1	1	0
	0	1	1	0	Slot 7	Bits 24-27		0	1	1	1
	0	1	1	1	Slot 8	Bits 28-31		1	0	0	0
	1	0	0	0	Slot 9	Bits 32-35		1	0	0	1
	1	0	0	1	Slot 10	Bits 36-39		0	0	0	0

Physical PSBAR	9	10	11	12	CCR	Box Tag Decode
	0	0	0	1	Bit 8	Frame 1 Valid
	0	0	1	0	Bit 9	Frame 2 Valid
	0	0	1	1	Bit 10	Frame 3 Valid
	0	1	0	0	Bit 11	Frame 4 Valid
	0	1	0	1	Bit 12	Frame 5 Valid
	0	1	1	0	Bit 13	Frame 6 Valid
	0	1	1	1	Bit 14	Frame 7 Valid
	1	0	0	0	Bit 15	Frame 8 Valid
	1	0	0	1	Bit 16	Frame 9 Valid
	1	0	1	0	Bit 17	Frame 10 Valid

Main Storage Select Switch	4	5	6	7	Switch Decode
	0	0	0	1	Decode SE1
	0	0	1	0	Decode SE2
	0	0	1	1	Decode SE3
	0	1	0	0	DEcode SE4
	0	1	0	1	Decode SE5
	0	1	1	0	Decode SE/DE6
	0	1	1	1	Decode SE/DE7
	1	0	0	0	Decode SE/DE8
	1	0	0	1	Decode SE/DE9
	1	0	1	0	Decode SE/DE10

Diagram 4-607. PSBAR Step Control Logic

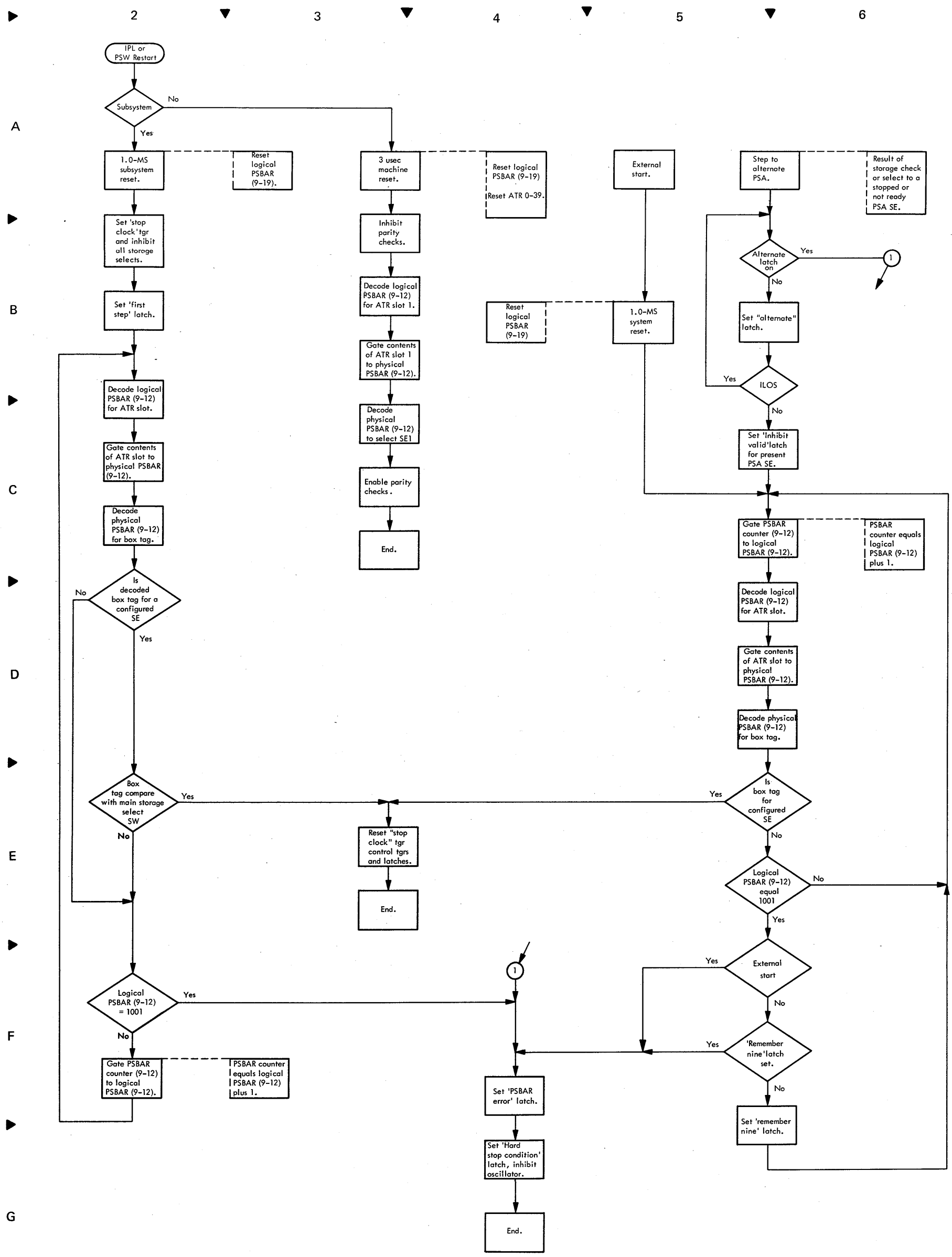


Diagram 4-608. PSBAR Operations

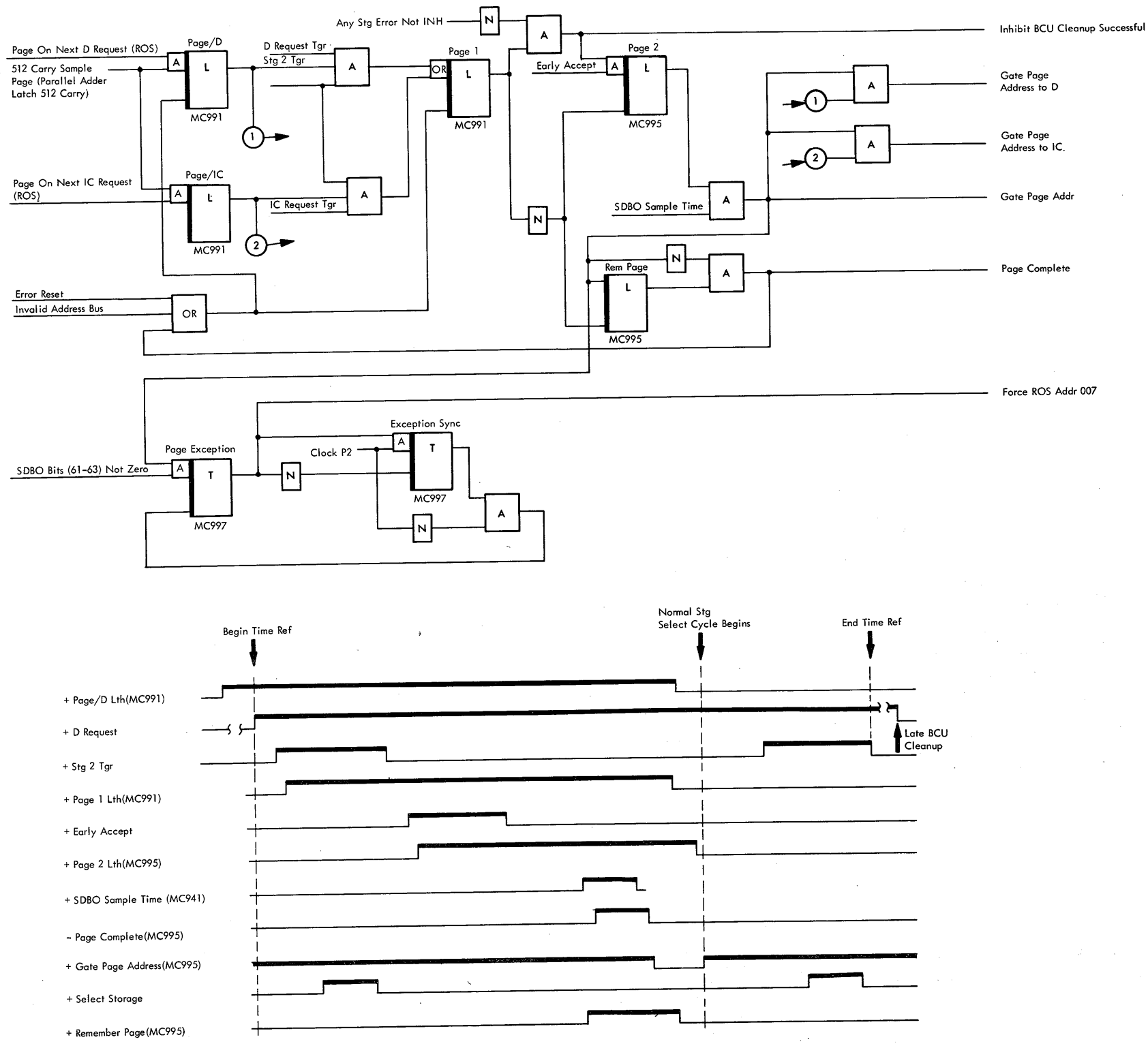


Diagram 4-609. Page Control Logic and Timing

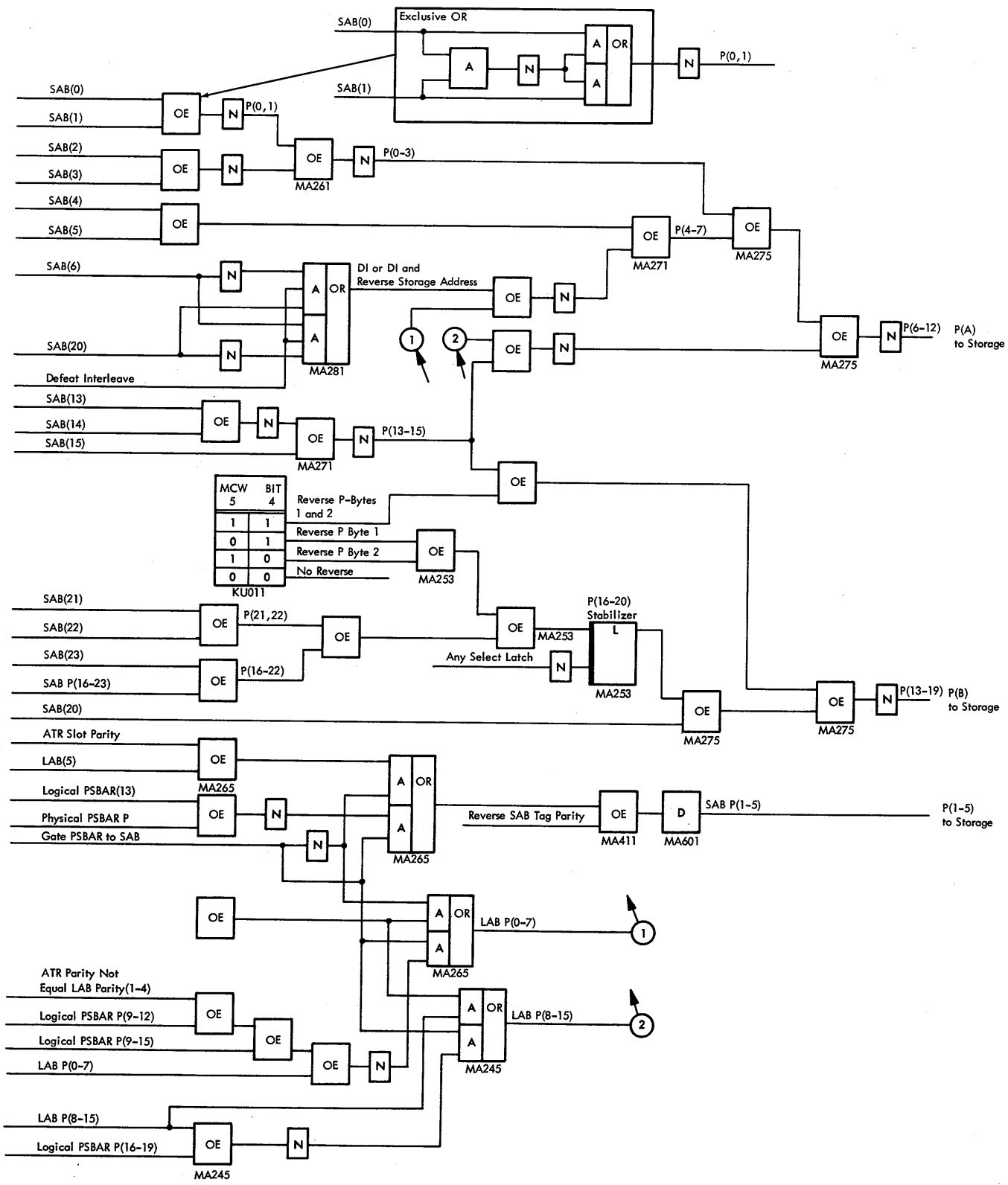


Diagram 4-610. SAB Parity Conversion Logic

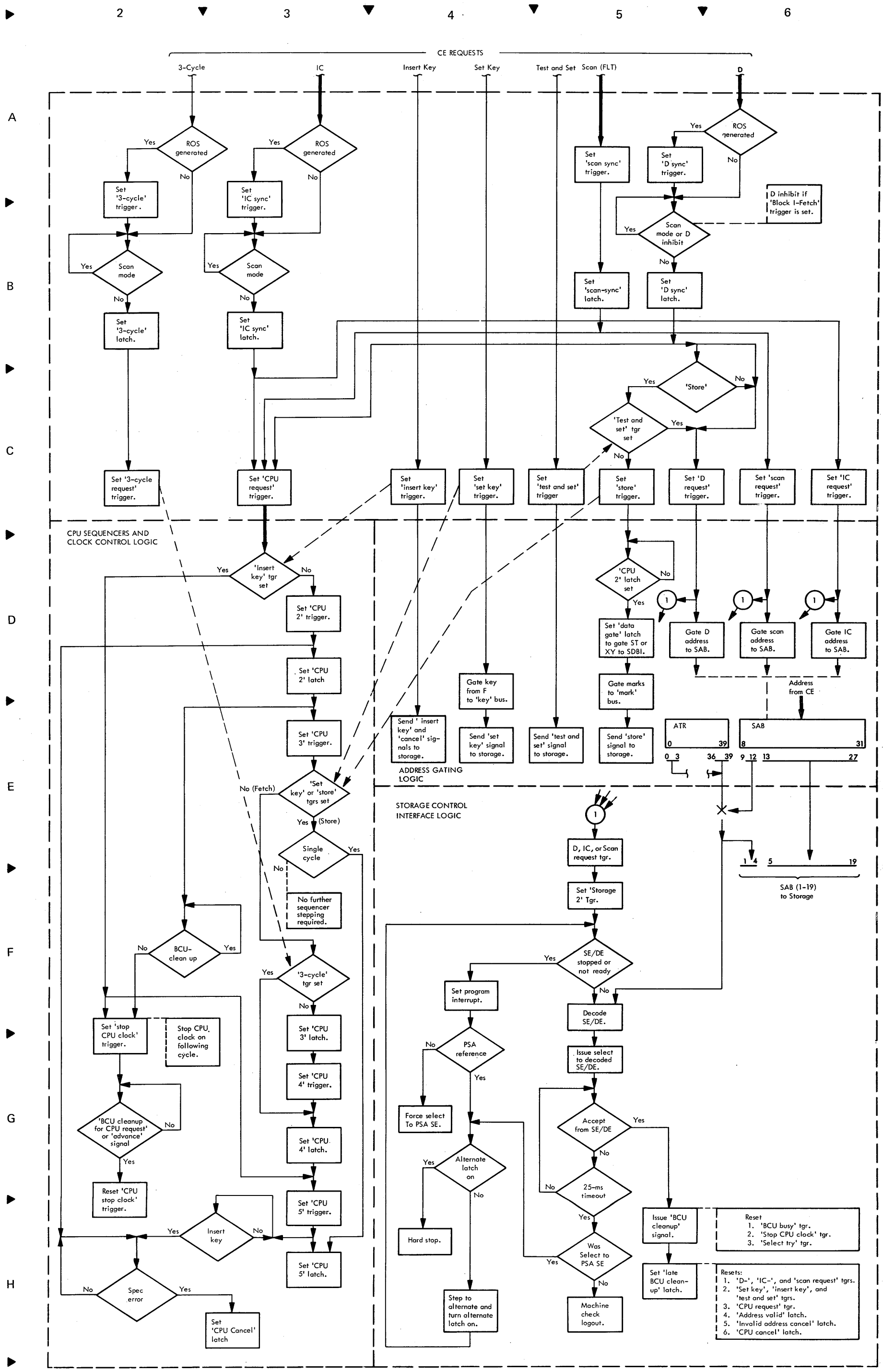


Diagram 4-611. Detailed SCI Functional Sequence (Sheet 1 of 2)

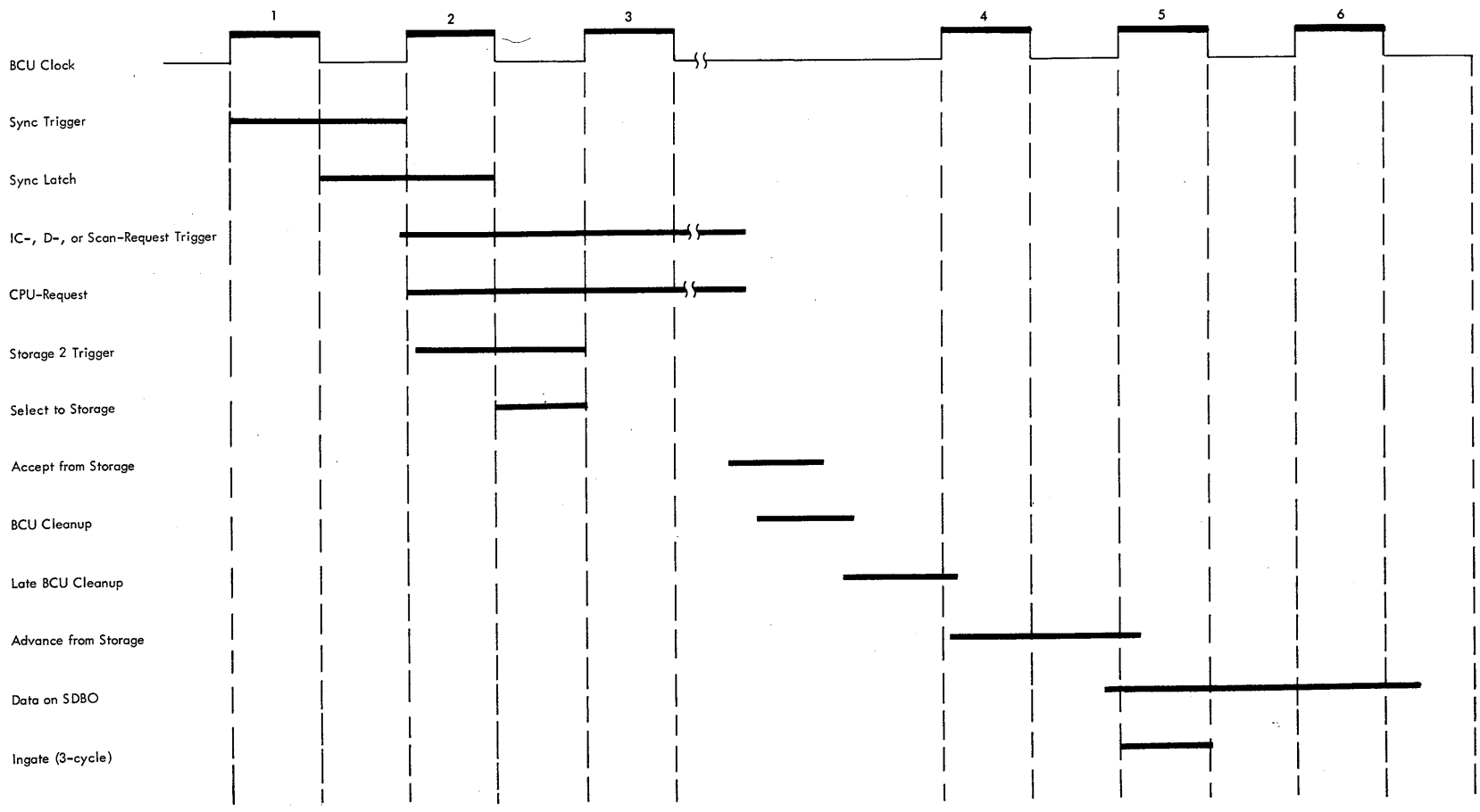


Diagram 4-611. Servicing of Storage Requests in Single-Cycle Mode (Sheet 2 of 2)

D

E

F

G

H

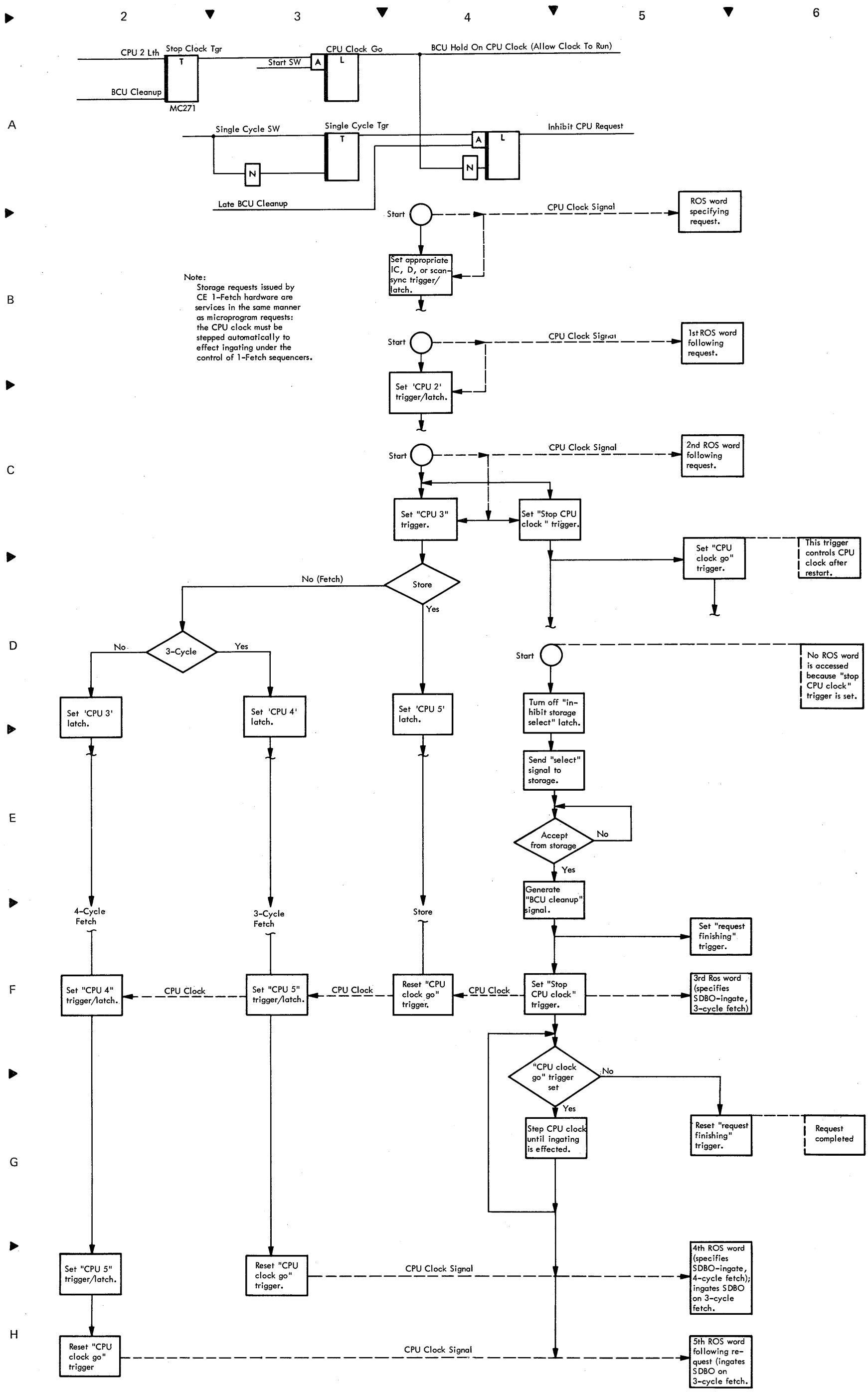


Diagram 4-612. Servicing of Storage Requests in Single-Cycle Mode